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DOSE RATE HARDNESS ASSURANCE GUIDELINES

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Technical Report

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This guideline develops an approach to Piece Part Hardness Assurance in the dose-rate environment. The guideline outlines two approaches based on the design margin for Piece Part used in the system. The first is modeled after the Design Margin Break Point method (DMBP) developed by the Air Force for systems with moderate requirements. It imposes a single criterion for design margin for all parts in the system. The second approach is a statistical approach, based on a log-normal distribution of part parameters, similar to the methods used in other hardness assurance guidelines. The discussion also includes some aspects of design hardening as they relate to the problem of dose-rate Hardness Assurance.

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PREFACE

Preparation of this guidelines document has been carried out under the direction of Defense Nuclear Agency, and their contracting officers Major B. Hickman and LCDR L. Cohn. Many individuals in the hardness assurance community have contributed significantly to the preparation of this document by preparing text, offering comments and reviewing draft documents. Special thanks must be given to Mr. J. Ferry (AFWL) who has served as the project monitor for this work; Dr. Eligius Wolicki who served as the DNA Program Area Reviewer for Hardness Assurance and the Chairman of the Space Parts Working Group Hardness Assurance Committee; and to Dr. Harvey Eisen, the present DNA Program Area Reviewer for Hardness Assurance. Special acknowledgment is given to William Alfonte (KAMAN-TEMPO), Tom Ellis (NWSC), Joseph Halpin (HDL), John Harrity (IRT), Alan Johnston (Boeing), George Messenger (DNA Consultant), Doug Millward (SAI), Arthur Namenson (NRL), Ron Pease (MRC), Robert Poll (JAYCOR) and Clay Rogers (JAYCOR) who have contributed significantly to the preparation of this document. Without the aid and expert knowledge of all of these individuals and the Hardness Assurance Committee of the NASA/SD Space Parts Group, the development of this document would not have been possible.

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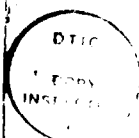
CONVERSION TABLE

Conversion factors for U.S. Customary to metric (Si) units of measurement

MULTIPLY ──────▶ BY ──────▶ TO GET
TO GET ◀────── BY ◀────── DIVIDE

angstrom	1.000 000 X E -10	meters (m)
atmosphere (normal)	1.013 25 X E +2	kilo pascal (kPa)
bar	1.000 000 X E +2	kilo pascal (kPa)
barn	1.000 000 X E -28	meter^2 (m^2)
British thermal unit (thermochemical)	1.054 350 X E +3	joule (J)
calorie (thermochemical)	4.184 000	joule (J)
cal (thermochemical)/cm^2	4.184 000 X E -2	mega joule/m^2 (MJ/m^2)
curie	3.700 000 X E +1	*giga becquerel (GBq)
degree (angle)	1.745 329 X E -2	radian (rad)
degree Fahrenheit	$t_K = (t°f + 459.67)/1.8$	degree kelvin (K)
electron volt	1.602 19 X E -19	joule (J)
erg	1.000 000 X E -7	joule (J)
erg/second	1.000 000 X E -7	watt (W)
foot	3.048 000 X E -1	meter (m)
foot-pound-force	1.355 818	joule (J)
gallon (U.S. liquid)	3.785 412 X E -3	meter^3 (m^3)
inch	2.540 000 X E -2	meter (m)
jerk	1.000 000 X E +9	joule (J)
joule/kilogram (J/kg) (radiation dose absorbed)	1.000 000	Gray (Gy)
kilotons	4.183	terajoules
kip (1000 lbf)	4.448 222 X E +3	newton (N)
kip/inch^2 (ksi)	6.894 757 X E +3	kilo pascal (kPa)
ktap	1.000 000 X E +2	newton-second/m^2 (N-s/m^2)
micron	1.000 000 X E -6	meter (m)
mil	2.540 000 X E -5	meter (m)
mile (international)	1.609 344 X E +3	meter (m)
ounce	2.834 952 X E -2	kilogram (kg)
pound-force (lbs avoirdupois)	4.448 222	newton (N)
pound-force inch	1.129 848 X E -1	newton-meter (N·m)
pound-force/inch	1.751 268 X E +2	newton/meter (N/m)
pound-force/foot^2	4.788 026 X E -2	kilo pascal (kPa)
pound-force/inch^2 (psi)	6.894 757	kilo pascal (kPa)
pound-mass (lbm avoirdupois)	4.535 924 X E -1	kilogram (kg)
pound-mass-foot^2 (moment of inertia)	4.214 011 X E -2	kilogram-meter^2 (kg·m^2)
pound-mass/foot^3	1.601 846 X E +1	kilogram/meter^3 (kg/m^3)
rad (radiation dose absorbed)	1.000 000 X E -2	**Gray (Gy)
roentgen	2.579 760 X E -4	coulomb/kilogram (C/kg)
shake	1.000 000 X E -8	second (s)
slug	1.459 390 X E +1	kilogram (kg)
torr (mm Hg, 0° C)	1.333 22 X E -1	kilo pascal (kPa)

*The becquerel (Bq) is the SI unit of radioactivity; 1 Bq = 1 event/s
**The Gray (Gy) is the SI unit of absorbed radiation.

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SECTION 1
INTRODUCTION

1.1 SCOPE.

The scope of this document is limited to dose-rate radiation effects on semiconductor electronics and is specifically intended to address hardness assurance at the piece-part level. Because the nature of dose-rate effects sometimes requires a close interaction between system hardness assurance and piece-part hardness assurance, some system requirements are also discussed.

1.2 OBJECTIVE.

1.2.1 Hardness Assurance.

Hardness assurance (HA) is the application of methods and procedures during the production phase of a system to ensure that the system retains the radiation hardness which it was designed to have. Although the principal application of hardness assurance is in the production phase, it is necessary to consider HA during the design phases of a program if a cost-effective system is to be obtained. Hardness assurance begins in the design phase with definition of the system requirements, radiation characterization of the piece-parts, calculation of the required design margins and the categorization of semiconductor parts.

Piece-part hardness assurance is the application of controls and tests to the procurement of an electronic part to ensure that its radiation response is within known and acceptable limits.

1.2.2 Design Hardening.

Radiation design hardening is the process in which circuit design, parts selection, and hardness assessment are performed to achieve an optimum and cost-effective circuit which will be survivable in a given radiation environment. In the design hardening process, the radiation response requirements for devices are determined and hardness criticality categorization takes place. With interaction between design hardening and hardness assurance activities, a cost-effective design can be obtained.

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1.2.3 Users of This Document.

This document is written primarily for those individuals who are involved with hardness assurance activities. It also provides a guide for designers of radiation hardened systems and, as a result, is an aid in developing hardness assurance design documentation (HADD).

1.2.3.1 Document Application. This document mainly discusses piece-part hardness assurance methods for the dose-rate environment, and addresses system hardness assurance topics only as they are necessary to complete the discussion of piece parts. Thus, the discussion will deal with the radiation categorizing of piece-parts according to certain criteria, which will determine the controls needed during part procurement. Specific activities and functions which may be significantly different for different systems and for different contracting organizations will not be discussed in detail in this document.

Many dose-rate-dependent problems, such as burnout and latchup, cannot effectively be handled at the piece-part level. In these cases, system- and/or circuit-level design solutions may be the most effective means of ensuring survival.

1.2.4 Failure Budget.

Dose-rate effects are never the only consideration for system survivability. Other effects such as aging, other nuclear radiation effects (e.g., those effects caused by total ionizing dose, neutron radiation, electromagnetic pulse (EMP), etc.), and other environmental effects (e.g., temperature) can also cause system failure.

Dose-rate effects are not generally associated with graceful degradation of a part or of the system. They are usually transient in nature and can be catastrophic to system survivability. Although there may be interactions between dose-rate effects and other environments (such as the effect of temperature on latchup, see section 5.2.2) the interaction is often difficult to quantify for purposes of allocating a failure budget. Nevertheless these interactions must be considered when characterizing parts and categorizing them for hardness assurance.

1.2.5 Environment.

Dose rate effects may be caused by a variety of ionizing radiation environments. These environments may consist of neutrons, photons, electrons, or single particle ionization. The methods which are used to harden against the various environments may vary from one environment to another. For example, shielding can be an effective tool for some low energy x-rays but may be ineffective for higher energy gamma rays. In contrast, even though the hardening methods may be different, one may find that the hardness assurance procurement procedures may be similar regardless of the environment.

1.3 RELATED DOCUMENTS.

This guideline document addresses dose rate effects in semiconductor electronic devices. It forms a part of a series of documents which discuss the problem of hardness assurance in military systems. Much of the background, mathematics and statistical analysis is covered in detail in other hardness assurance documents and therefore is not repeated here. In particular, the approach used in this document is based on the methods developed in two hardness assurance guideline documents which were developed for the neutron and total dose environments. Every attempt has been made to keep the definitions and procedures consistent with the two published documents (Refs 1,2).

Documents Relevant to Hardness Assurance.

Specification

Military

MIL-S-19500   Semiconductor Devices, General Specifications for

MIL-M-38510   Microcircuits, General Specifications for

MIL-C-45662   Calibration System Requirements

Standards

Military

MIL-STD-202   Test Methods for Electronic and Electrical Component Parts

MIL-STD-750   Test Methods for Semiconductor Devices

MIL-STD-883   Test Methods and Procedures for Microelectronics

ASTM

ASTM-E665-78	Standard Practice for Determining Absorbed Dose versus Depth in Materials Exposed to the X-Ray Output of Flash X-Ray Machines
ASTM E 666-78	Standard Method for Calculation of Absorbed Dose from Gamma or X Radiation
ASTM E 668-78	Standard Practice for the Application of Thermoluminescence-dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation Hardness Testing of Electronic Devices
ASTM E 820-81	Standard Practice for Determining Absolute Absorbed Dose Rates for Electron Beams
ASTM F 448-80	Standard Method for Measuring Steady-State Primary Photo-current
ASTM F 675-80	Standard Method for Measuring Nonequilibrium Transient Photocurrents in P-N Junctions
ASTM F 744-81	Standard Method for Measurement of Dose Rate Threshold for Upset of Digital Integrated Circuits
ASTM F 773-82	Standard Method for Measuring Dose Rate Response of Linear Integrated Circuits
ASTM F 526-77	Method of Dose Measurement for Use in Linear Accelerator Pulsed Radiation Effects Tests

Guidelines and Reports

DNA 5910F	Piece-Part Neutron Hardness Assurance Guidelines for Semi-conductor Parts (MIL-HDBK-280)
DNA 5909F	Total Dose Hardness Assurance Guidelines (MIL-HDBK-279)
DNA 5928	Latchup Analysis of Bipolar Integrated Circuits
DNA 5915	Upset Response Testing of MSI Integrated Circuits

Military Handbooks

MIL-HDBK-279	Total Dose Hardness Assurance Guidelines (DNA-59009F)
MIL-HDBK-280	Piecepart Neutron Hardness Assurance Guidelines for Semi-conductor Parts (DNA 5910F)

SECTION 2
DEFINITIONS, SYMBOLS, AND ABBREVIATIONS

2.1 DEFINITIONS.

Burnout is the failure of a device subjected to electrical overstress. Typically, thermal damage has occurred within one or more device junctions or within the device metallization.

Confidence Level (C) is the probability (usually given in percent) that at least a portion, P_{DIST}, of the parts in the lot will survive.

Cumulative Probability (P_{DIST}) is the percentage or proportion of a probability distribution which is below a given upper limit (or above a given lower limit).

Design Margin Break Point (DMBP) is a categorization method which provides a criterion which may apply to all parts in a system and is based on a single fixed value of design margin.

Dose Rate ($\dot{\gamma}$) is the dose rate level under consideration. It is usually stated in terms of rad(Si)/sec.

Dose Rate Design Margin (DM$\dot{\gamma}$) is the ratio of the mean failure dose rate to a specified dose rate.

Dose Rate to Failure Value ($\dot{\gamma}_{FAIL}$) is the dose rate level for the part under test at which a parameter designated as PAR_{RAD} equals PAR_{FAIL}.

Hardness Assessment is the determination of the susceptibility to damage or upset of a system, subsystem or component.

Hardness Assurance consists of the procedures, controls, and tests applied during system design, fabrication, and procurement to ensure that the system has a response to nuclear radiation that is within known and acceptable limits.

Hardness Assurance at the piece-part level is the application of controls and tests to the procurement of an electronic part to ensure that its radiation response is within known and acceptable limits.

Hardness Maintenance is the combination of inspection, test, and repair activities accomplished on a hardened system to ensure that the hardness built into the system is retained throughout the system lifetime.

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Hardness Surveillance consists of the long term inspection and test procedures, performed beyond hardness maintenance, which are conducted to assure that systems are, in fact, being properly maintained with the desired hardness.

Hardness Verification is the determination through a careful sequence of tests and analyses that a system design is in fact hardened in compliance with the nuclear specification.

Latchup in integrated circuits is an abnormal operating state usually characterized by the failure of a device to respond properly to input conditions, and/or the presence of abnormally high currents flowing in the device. Latchup is usually caused by the regenerative action of four layer (PNPN) conduction paths within the device.

Lot is the collection of parts from which the sample has been taken (see MIL-M-38510).

Lot Acceptance Test is the test of a sample of parts from a procurement lot to determine if the lot is acceptable. For the purpose of Hardness Assurance, this term is intended to be a generic term in order to standarize on commonly used expressions such as Lot Conformance Test, Quality Conformance Test, or Quality Conformance Inspection.

Lot Size (N) is the number of parts in the lot before the sample has been removed.

Mean Dose Rate to Failure $(\dot{\gamma}_{MF})$

$$\dot{\gamma}_{MF} \equiv \exp\overline{\left[\ell n(\dot{\gamma}_{FAIL})\right]} \tag{1}$$

Measured Logarithmic Mean for PAR$_{RAD}$ $\overline{\left[\ell n(PAR_{RAD})\right]}$

$$\overline{\ell n(PAR_{RAD})} \equiv \frac{1}{n} \sum_{i=1}^{n} \ell n(PAR_{RAD_i}) \tag{2}$$

where PAR_{RAD_i} is PAR_{RAD} for the ith device.

$\ell n(PAR_{RAD})$ is useful for log-normally distributed variables.

Measured Logarithmic Mean for $\dot{\gamma}_{FAIL}$ $\left[\overline{\ln(\dot{\gamma}_{FAIL})}\right]$

$$\overline{\ln(\dot{\gamma}_{FAIL})} \equiv \frac{1}{n} \sum_{i=1}^{n} \ln(\dot{\gamma}_{FAIL_i}) \tag{3}$$

where $\dot{\gamma}_{FAIL_i}$ is the $\dot{\gamma}_{FAIL}$ for the ith device.

Measured Logarithmic Standard Deviation for $\dot{\gamma}_{FAIL}$ $\left[s_{\ln(\dot{\gamma}_{FAIL})}\right]$

$$s_{\ln(\dot{\gamma}_{FAIL})} \equiv \left\{ \frac{1}{n-1} \sum_{i=1}^{n} \left[\ln(\dot{\gamma}_{FAIL_i}) - \overline{\ln(\dot{\gamma}_{FAIL})} \right]^2 \right\}^{1/2} \tag{4}$$

Measured Logarithmic Standard Deviation for PAR_{RAD} $\left[s_{\ln(PAR_{RAD})}\right]$

$$s_{\ln(PAR_{RAD})} \equiv \left\{ \frac{1}{n-1} \sum_{i=1}^{n} \left[\ln(PAR_{RAD_i}) - \ln(\overline{PAR_{RAD}}) \right]^2 \right\}^{1/2} \tag{5}$$

Measured Mean for PAR ($\overline{PAR}$)

$$\overline{PAR} \equiv \frac{1}{n} \sum_{i=1}^{n} PAR_i \tag{6}$$

where PAR_i is the parameter value measured for the ith device.

Measured Standard Deviation for PAR_{RAD} $\left[s(PAR_{RAD})\right]$

$$s(PAR_{RAD}) \equiv \left\{ \frac{1}{n-1} \sum_{i=1}^{n} (PAR_{RAD_i} - PAR)^2 \right\}^{1/2} \tag{7}$$

One-Sided Tolerance Limit (K_{TL}) is the number of standard deviations from the mean which defines a limit on a normally distributed parameter (PAR), with confidence C that the parameter in the parent population is greater than

$$PAR - K_{TL}(n,C,P_{FAIL})*S(PAR) \tag{8}$$

or less than

$$PAR + K_{TL}(n,C,P_{FAIL})*S(PAR) \quad .$$

Parameter Failure Value (PAR_{FAIL}) is the value of a particular parameter for the device under evaluation at which circuit failure is defined to occur. This value is application dependent.

Parameter Specification Value (PAR_{MIN} or PAR_{MAX}) is the specified minimum or maximum device parameter value prior to irradiation. This value is usually given by the manufacturer.

Parameter Design Margin (DM)

$$DM = PAR_{FAIL}/\exp\left[\overline{\ln(PAR_{RAD})}\right] \tag{9}$$

for parameters which increase with radiation, and

$$DM = \exp\left[\overline{\ln(PAR_{RAD})}\right]/PAR_{FAIL} \tag{10}$$

for parameters which decrease with radiation, where PAR_{RAD} is evaluated at $\dot{\gamma}_{SPEC}$.

Part (Piece Part) is the electronic device used in a specific circuit application or test.

Part Categorization Criterion (PCC) is a categorization method which sets a separate criterion to categorize each particular part type used in a system. The DM of each part type is compared to its PCC to determine its part category.

Part Parameter Value (PAR) is the electrical parameter value measured for a device.

Radiation-Induced Parameter Value (PAR_{RAD}) is the value of a parameter at a particular radiation level.

Sample Size (n) is the number of parts, selected at random from the lot, to be tested.

Specified Dose Rate ($\dot{\gamma}_{SPEC}$) is the maximum dose rate which the circuit under consideration must withstand.

Survivability Level is the radiation level which the device, circuit or system can withstand without suffering an impairment of its ability to accomplish its function.

Vulnerability Level is the level at which the device is considered to have failed the functional requirement.

2.2 SYMBOLS.

C	Confidence level
DM(PAR)	Parameter design margin
DMBP	Design margin break point
DM	Dose rate design margin
$\dot{\gamma}_{FAIL}$	Dose-rate-to-failure value
$\dot{\gamma}_{MF}$	Mean dose rate to failure
$\dot{\gamma}_{SPEC}$	Specified dose rate
$\dot{\gamma}_{CIRC}$	Circumvention dose rate
I_p	Junction photocurrent
I_{pp}	Primary photocurrent
I_s	Circuit saturation current
I_{sp}	Secondary photocurrent
I_T	Terminal current
I_{TH}	Threshold current
K_{TL}	One-sided tolerance limit factor
$\ln(PAR_{RAD})$	Measured logarithmic mean for PAR_{RAD}
$\ln(\dot{\gamma}_{FAIL})$	Measured logarithmic mean for $\dot{\gamma}_{FAIL}$
n	Sample size
N	Lot size

PAR	Device parameter value
PAR_{FAIL}	Parameter failure value
PAR_{MIN} or PAR_{MAX}	Specified parameter value (minimum or maximum)
PAR_{RAD}	Radiation-induced parameter value
PCC	Part categorization criterion
P_{DIST}	Cumulative proportion of distribution
$s_{ln(PAR_{RAD})}$	Measured logarithmic standard deviation for PAR_{RAD}
$s_{ln(\dot{\gamma}_{FAIL})}$	Measured logarithmic standard deviation for $\dot{\gamma}_{FAIL}$
t_{rec}	Recovery time
t_{spec}	Allowable recovery time

2.3 ACRONYMS.

CCB	Configuration Control Board
HA	Hardness assurance
HADD	Hardness assurance design oocumentation
HCC	Hardness critical category
HCI	Hardness critical item
HM	Hardness maintenance
HNC	Hardness non-critical
PMPCB	Parts, material and process control board
SPO	System Project Office. The SPO is the overall controlling organization for the project under consideration. It is intended to be a generic term so as to standardize, for the purposes of this document, such expressions as system, system project, Project Manager's Office, Project Manager, procurement agency, and contracting agency.

SECTION 3
OVERVIEW

3.1 OVERVIEW OF DOSE-RATE HARDNESS ASSURANCE.

This section is intended to provide a brief overview of the important elements of dose-rate hardness assurance. The following sections of the document will address some of these issues in greater detail.

The dose-rate environment produces transient current surges in semiconductor devices. In a single junction, the current is called photocurrent (I_p) and flows in the direction of junction leakage current. In transistors, the current surge in the collector-base junction is called the primary photocurrent (I_{pp}) and may, in certain cases, be amplified by the transistor gain to produce secondary photocurrents (I_{sp}).

In discrete devices, these currents may appear as a transient noise pulse, interfering with the normal operation of the device or the circuit in which it is used. If the radiation is intense enough and if the resulting energy deposited in the device is great enough, the device may burn out.

Dose-rate effects in integrated circuits are similar to the effects observed in discrete devices. One common term which is used to describe the dose-rate effect in integrated circuits is "upset." The device is said to have upset when the dose-rate effect results in the device being in an unwanted operating state as a result of the radiation. For example, the dose rate response of bipolar linear circuits may appear as an output voltage transient lasting up to 10 or more microseconds, along with power supply surge currents. Digital circuits may experience a change in output state, a single or multiple cell change of state (bit flip), or simply a deviation in output voltage which is defined as being unacceptable for proper operation of the device. In most cases, the device usually will recover and continue to function normally, once it is returned to its correct operating condition. However, if sufficient energy is available, the device may be damaged and may not recover after the radiation pulse.

In both linear and digital integrated circuits, the device may experience an effect called four-layer latchup. Should the device enter a latchup condition, the circuit will cease to respond to input signals, and may in fact burn out. A summary of these effects is shown in Figure 1.
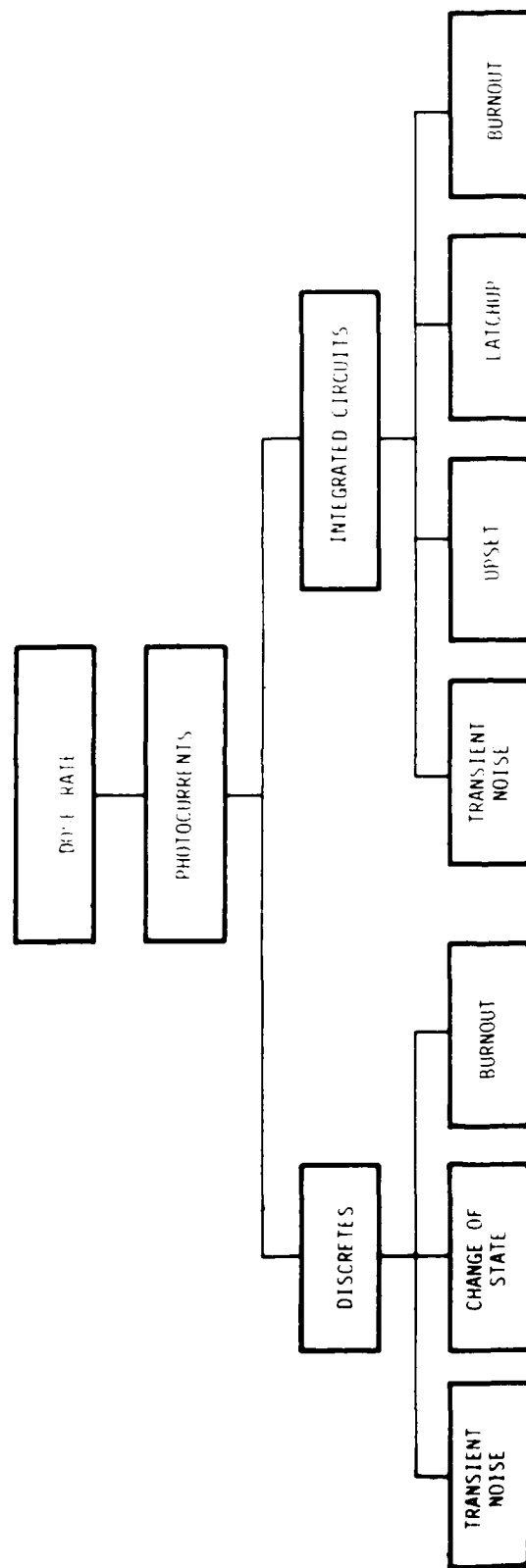
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Figure 1. Response tree for dose-rate effects.

The following sections describe those specific aspects of design hardening which affect dose-rate hardness assurance and outline the general requirements for radiation design hardening. The output of the design hardening program as required for hardness assurance is discussed.

3.2 OVERVIEW OF DOSE-RATE DESIGN HARDENING.

Dose rate design hardening is the iterative process by which the system requirements are assessed, the circuits are designed, parts are selected, and circuit susceptibility is assessed to achieve an optimally hardened circuit design. The system specifications are met by hardening methods such as part selection, current-limiting, photocurrent compensation, power management, shielding, and other methods.

In this process, candidate device types are evaluated for their susceptibility to the dose rate environment. Existing threshold data for the devices is used if those data are judged to be of satisfactory quality; otherwise, new characterization data must be obtained.

The process is complicated by the fact that a wide variety of effects exist for the dose-rate environment. Upset is usually nondestructive and thresholds may be precisely determined. Burnout is destructive, difficult to measure, and statistically uncertain and, therefore, is less precisely determined. Latchup is usually a low-occurrence failure mode and the dose rate thresholds for most devices are usually much too difficult to measure within a part type. Nevertheless, the most important outcome of the design hardening process is to categorize the parts into one of the following categories.

- Unacceptable parts -- parts with a dose rate susceptibility threshold so extremely low that further circuit hardening or the cost and risk of hardness assurance methods are judged to be unacceptable.

- Hardness Critical Category 1 parts (HCC-1) -- those parts which require special hardness assurance procedures to be acceptable.

- Hardness Critical Category 2 parts (HCC-2) -- those parts in which the dose rate susceptibility thresholds exceed the radiation requirements by a large enough margin so that no further testing is judged to be required on a lot by lot basis. An occasional sample test may be required on some interval, (e.g., an arbitrary interval of three to six months)[*] to assure that the hardness level of the device has not degraded.

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[*] The actual interval may depend on factors such as design margin, part variability, experience with part, engineering judgement, etc.

- Hardness Non-Critical (HNC) -- those parts which by virtue of their inherent hardness require no further testing.

It should be noted that the parts must be categorized separately for each dose-rate radiation effect. For example, a dielectrically isolated integrated circuit may be judged to be HNC for latchup but a HCC-1 for upset. Therefore, the device would be categorized as HCC-1.

3.3 DOCUMENTATION.

Hardness assurance for piece parts takes place during the system production and parts procurement phases. The tests and screens which were determined during the design phase, and are described in detail in the hardness assurance design documentation (HADD), are put into effect during the hardness assurance phase.

The hardness assurance design documentation (HADD) is a collection of information on the design hardening techniques used, the survivability/vulnerability analysis, configuration and quality control, test data, procurement specifications, management and any other information necessary for production of the system.

These documents may vary between systems, but a common set would contain the following:*

a. Volume 1, Introduction. This volume provides a general systems operation and functional description.

b. Volume 2, HCI Index. This volume provides a hardness critical item list which relates hardness critical parts to their application. The hardness criticality is indicated and cross-referenced to analysis.

c. Volume 3, Hardness Assurance Plan. This volume presents the management organization and technical requirements which are to be implemented throughout the production period.

d. Volume 4, Analysis Volumes. These volumes contain the survivability/vulnerability analysis and any related information.

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*For a more complete description of the HADD, see Ref. (3).

SECTION 4

DETAILED REQUIREMENTS FROM DESIGN HARDENING

4.1 RADIATION DESIGN HARDENING.

The purpose of this section is to point out some of the more important factors in radiation design hardening as they apply to hardness assurance. Since the dose-rate environment can cause both transient and permanent effects in devices, hardening electronic circuits against these effects may take many forms. It is not the intent of this section to discuss design hardening in detail. A complete discussion is beyond the scope of this document. However, it is the intent to point out some of the important aspects of design hardening that apply or have outcomes important to hardness assurance.

Dose-rate hardening methods cannot usually be limited to a single technique which applies to all effects. In addition, many of the techniques used involve circuit or system-level consideration and do not necessarily depend on specific device characteristics. In general, hardening techniques fall into three categories.

1. Those which deal with the devices themselves and, therefore, are strongly influenced by the choice of devices (e.g., dielectric isolation).

2. Those which use a circuit or system solution that depends on knowledge of the device characteristics, (e.g. current limiting).

3. Those which use a circuit or system solution that does not directly depend on the specific device characteristics, (e.g. circumvention).

Once system analysis has been performed and it has been determined that dose-rate hardening is required, the process of design hardening begins and must produce several results which are important for the hardness assurance program. The following are those required to carry out a successful program.

1. Parts selection and hardening measures.

2. Determination of the circuit failure criterion for each part application and dose-rate effect on the basis of worst-case analysis.

3. Determination of the mean-dose-rate-to-failure which causes the circuit or device to fail.

4. Identification of the characterization data, data source, and quality of data used for the determination of failure.

5. Determination of the device design margins.

6. Determination of the part categorization criteria, PCC, or the DMBP value. The device design margins are compared to the categorization criteria to determine test and control criteria.

7. Categorization of the part for each application and effect being evaluated.

In some cases, where little data are available, part characterization may be used to qualify devices on a statistical basis. Statistical qualification requires that the population of devices has a statistically well behaved dose-rate response which follows a known distribution. In other situations where the part response is extremely variable, a worst-case estimate of the bound of the statistical distribution may be used.

Part types with very small design margins should be eliminated from use in the system. The decision as to when a design margin is small enough to make the part unacceptable will depend on the cost of rejecting lots during hardness assurance versus the cost of either using a less sensitive part type or redesigning the circuit. Since these costs are highly dependent on the specific part type and the specific system in which the part is used, no one formula for determining a minimum acceptable design margin can apply to all situations. Two suggested general rules for selecting parts are:

1. Part types with design margins 1 or less will not be used.

2. Part types with design margins between 1 and 2 are generally unacceptable, and should be used only if no alternatives are available. On the basis of calculations for silicon bipolar transistors, a relatively high rate of lot rejection and/or part failure is to be expected when parts with design margins less than 2 are used. The actual rejection rate and risk will depend on the part distribution and the variance of that distribution.

4.1.1 Part Selection.

During design hardening, one of the most effective steps for reducing hardness assurance costs is the proper selection of radiation-resistant parts. This is particularly important for dose-rate effects, since some of these effects are most efficiently handled by the choice of proper parts.

Device design fabrication parameters may be an important factor in controlling the dose-rate response of a device. For example, parts with dielectric isolation, gold doping, buried layers or other techniques, may be used to avoid latchup. Internal photocurrent compensation may be used to improve the threshold for upset. These kinds of factors need to be considered when components are being selected. Parts with smaller geometry, having lower photoresponse, might be substituted for parts with unacceptably large photoresponse. Parts with higher thresholds for upset or burnout may be substituted for others.

4.1.2 Circuit Design Features.

The use of special circuit design features may be an effective system solution to accomplish hardening for the dose rate environment. The use of low voltages and long circuit time constants may be an effective hardening method. Low voltages reduce the probability of latchup, while long circuit time constants may raise the upset threshold of the device.

Current limiting is a hardening technique which, through circuit design, limits the maximum current which may be delivered to the device. In general, current limiting can be an effective means of increasing the immunity of the device to burnout. In some cases it may also be effective in latchup control.

4.1.3 System Level Solutions.

Like part selection, circuit design hardening can be a very effective way of reducing the hardness assurance effort. Again, if a circuit can be redesigned to change the classification of a part from radiation sensitive to insensitive, such redesign may be highly cost-effective over the life cycle of the system. Although the subject is very complex and a complete treatment is beyond the scope of this document, the following suggestions may be considered.

1. Where possible, circuits should be designed so as to maximize the use of intrinsically-hard parts, and to minimize the use of costly radiation hardened parts.

2. Circuits should be designed to minimize sensitivity to the transient dose-rate response.

3. Limiting resistors should be used to protect devices from burnout and to reduce latchup sensitivity.

4. System or circuit design solutions should be considered for devices where a design margin approach is not possible. For example, devices that are susceptible to latchup do not usually lend themselves to a design margin approach. In this case a power management technique, where power is momentarily removed, would be a possible alternative at the system level.

4.1.3.1 Circumvention and Power Management. It is not always feasible to eliminate all devices which are latchup-prone from the system design. Therefore, the danger of device latchup must be eliminated by other means. Often, some form of power management is used in circuit design. Either the power is periodically removed from the device through a method of power strobing, where the device power is periodically removed; or power is removed upon the detection of radiation, as in circumvention.

4.1.3.2 Fault-Tolerant Design. The area of fault-tolerant design is beyond the scope of this document. For the present, it is sufficient to note that some circuits are able to tolerate the upset or failure of some devices. In upset-tolerant circuits, the devices are usually linear or combinatorial logic devices and are restored to their correct operating conditions after the radiation pulse. Man-attended equipment may even be allowed to tolerate latchup, blown fuses and tripped circuit breakers.

4.1.3.3 Shielding. For space systems, prompt dose-rate effects are the result of the sum of the x-ray and prompt gamma-ray induced transient ionization. The dose rate caused by the x-rays is usually dominant over the gamma-ray dose rate. The x-ray dose rate can sometimes be reduced with shielding to a level where combined x-ray and gamma-ray dose rates will not cause damage to the system. The gamma-ray environment cannot practically be reduced with shielding for missile or airborne systems. For systems which must operate through an event, this can be important since the gamma rays alone can induce circuit upset. It should be noted that some shields used to reduce the x-ray dose can cause IEMP problems and techniques such as using low-Z coating material may be required to reduce electron emission on certain space or airborne systems. For some ground-based systems, large amounts of shielding may be possible. Concrete bunkers or other heavy shields may be considered.

In many space systems, dose-rate effects can be greatly reduced through the use of some careful design factors and judicious shielding. Some simple design rules that are often used are:

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1. Bury sensitive components deep in the system, for self-shielding.

2. Group sensitive components together for mutual protection and shadowing and more economical shielding.

3. Locate such groupings near massive structural elements.

4. Increase chassis and structural element thickness in selected areas for increased shielding.

5. Include small local device shields for additional dose rate reduction.

It is important to note that the weight penalty for extensive and massive shielding is often prohibitive for space or airborne systems, and device location is often dictated by circuit requirements which may preclude locating the part in an optimum location for shielding. New packaging techniques are being developed, which incorporate shielding as part of specially constructed packages (Ref. 4).

4.2 PART CATEGORIZATION METHODS.

As part of the design phase, it is necessary to determine the radiation response of the part types, and to classify the parts with regard to the need for hardness assurance. The categorization of the part types is performed in accordance with Section 5.

Categorization of parts is more complex for dose-rate effects than for other radiation effects. Because of the multiplicity of effects in the dose-rate environment, each effect should be considered separately. For example, a part may be protected from burnout by providing adequate current-limiting but may still be sensitive to upset. Thus, the part would be examined for each failure mode identified in the design.

Fortunately, some failure modes such as upset are nondestructive and, therefore, may be handled using a 100% screen to ensure hardness. However, such screens may be necessary only in the most severe environments where the parts have a small margin, or for special cases such as radiation detectors.

The categories into which parts may be segregated based on their various dose rate responses are:

Hardness Critical Category 1M (HCC-1M)   Lot acceptance tests and/or hardness assurance screens required.

Hardness Critical Category 1S (HCC-1S)   These parts may not require lot acceptance tests because they have sufficient design margin, but are included in the HCC-1 classification because they may

be nonstandard parts, or may require special procurement from one or more specific manufacturers due to the particular process-related radiation characteristics of the manufacturers. HCC-1S parts may require occasional sample testing similar to that which may be done for HCC-2 parts, to assure that the process-related radiation characteristics do not change with time.

Hardness Critical Category 1H (HCC-1H) — These parts would not require lot acceptance tests on the basis of design margin, but are included in the HCC-1 classification because they are hardness-dedicated parts. These parts are included in the design for the purpose of hardening. Protection diodes and circumvention detectors are in this category.

Hardness Critical Category 2 (HCC-2) — These parts do not require lot acceptance tests, but may require occasional sample testing to verify that the manufacturing process has not changed significantly.

Hardness Noncritical (HNC) — These parts have such large design margins, or do not have a critical radiation failure criterion, so that testing is not required, even on an occasional basis.

Design margins are used to categorize parts to determine the degree of control and testing that may be required. Two methods are proposed for classifying the parts. Both methods require part radiation characterization test data to determine a design margin. The design margin is then compared to a numerical value specified by one of the two methods.

The first method is the design margin breakpoint (DMBP) method (Ref. 3), in which the dose-rate design margin is compared to the DMBP value. A single DMBP value is specified during the design phase and applies to all devices in the system. This method is generally useful where the radiation environment is not severe with respect to expected device hardness.

In the second method, the design margin is compared to a number determined separately for each part type by analyzing the individual characterization data for each type. This method is called the part categorization criteria (PCC) method, and can be applied to all effects.

In addition to the DMBP and PCC values, the design developers may specify a level above the specification criteria requirements that is used to differentiate between unacceptable parts and those classified as HCC-1M. The value assigned to this number is based on several considerations. A small value may be desirable to minimize the number of part types categorized as unacceptable. However, too small of a value may result in an unacceptably high rejection rate during lot acceptance testing for part

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types with small design margin values. The value selected will be a compromise between these two factors.

4.2.1 Design Margin Break Point Method.

The DMBP method (Ref. 3) is generally most useful for systems with moderate requirements. When the DMBP method is used, a single value of the DMBP is specified during the design phase. This number is the breakpoint between HCC-1M, where tests are required on each lot, and HCC-2, where tests are not required on each lot. In addition, a design margin which separates HCC-2 from HNC will also be specified.

The DMBP value is generally thought to represent an arbitrary survival probability and confidence level. Increasing this value increases the confidence that can be placed in the HCC-2 part categorization. However, it also increases the number of HCC-1M part types that will require lot acceptance testing. Generally, it is cost-effective to set the DMBP value as low as practical within the risk factors established by the system requirements. The DMBP method is important for dose-rate hardness assurance because statistical failure distributions are not known for all effects, and the designer must more strongly rely on engineering judgment. A design margin breakpoint value will need to be specified on the basis of the best available information.

4.2.2 Part Categorization Criteria Method.

The PCC method (Refs. 1,2) is most often used for systems with severe requirements. However, one of the more important assumptions made in using the PCC method is that the failure response of the device may be characterized by a known, or perhaps a worst-case, statistical distribution. Before the methods used to determine the part categorization are presented, it should be pointed out that a significant portion of radiation test data seems to be best represented by the lognormal statistical distribution. (The lognormal distribution is non-symmetrical, with a positively skewed tail.) The mean value for this distribution is the geometric mean, and the variance of the data is the geometric dispersion. To apply normal statistical calculations to lognormal data, it is first necessary to transform the data into a normal distribution space by taking the logarithm of the data. After the normal statistical calculations are completed, the antilogs must be used to transform the calculations back into the lognormal space (Refs. 1,5).

It is believed that some dose-rate effects do not follow lognormal statistics. It has been suggested that some burnout data may follow a bimodal distribution (Ref. 6).

Therefore, before these hardness assurance methods are applied, one must ensure that the statistics being used to define the hardness assurance tests adequately describe the observed data though standard statistical tests. In some cases, a larger design margin may be indicated and the DMBP method may be used to compensate for distributional variations.

4.3 WORST-CASE ANALYSIS.

The dose-rate environment produces a transient photoresponse in semiconductor devices which results in a variety of device effects, depending on the type of device. The design margin, on the other hand, is usually defined in terms of the ratio of the mean dose-rate (at which the parametric change is equal to the design tolerance), to the criterion level. The important point is that the design margin is usually defined as the ratio of a mean failure dose-rate level to a specified level.

Although the actual design margin may be defined in terms of a dose-rate margin, the actual failure occurs when a particular device parameter reaches some limit. This end-point electrical parameter failure value is called PAR_{FAIL} and is determined by worst-case circuit analysis.

Since dose-rate effects are often transient in nature, the actual failure parameter may not be one of the usually measured device parameters such as gain or saturation voltage. The dose rate effect may be an upset, change in output voltage, or even a device burnout. Table 1 gives a partial list of some common dose-rate effects for a number of device types.

4.3.1 Upset Analysis.

Upset is a nondestructive transient effect that interrupts normal system operation. Circuit upset may or may not occur because of device photocurrent, depending on the circuit and piece-part response and recovery time. Hardening against upset can require circuit modification e.g., increasing circuit time constants, software modification, signal time sequencing, or piece-part replacement.

The use of piece-part photocurrent data is frequently limited in upset analysis to comparison of circuits and devices as a first-cut screen to identify critical circuits that require detailed analysis and further test data. Existing piece-part photocurrent data often must be interpolated or extrapolated because the radiation levels or pulsewidths used to obtain the data are not the same as those of the specified environment. Extrapolation of photocurrent data to higher radiation levels can lead to large errors because effects become nonlinear (e.g., the device may saturate).

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Table 1. Typical dose-rate failure parameter criteria for several device types.

Part Class	Parameter	Failure Condition and Comments
Diode	I_p = photocurrent	$I_p = I_{th}$ where I_{th} is the pulsed power damage threshold.
Transistor	I_s = saturation current	$I_s = I_{th}$ or
	I_{sp} = secondary photocurrent	$I_{sp} = I_{th}$
Linear ICs	Transient Upset	$t_{rec} = t_{spec}$
	Burnout	$I_T = I_{th}$
	Latchup	Latchup cannot be handled in terms of a PAR_{FAIL}. Device ceases to respond.
Digital	Upset	ΔV_0 change in output V Upset may be handled in terms of noise margins, or simply in terms of the dose rate which produces upset.
	Burnout	$I_T = I_{th}$
	Latchup	Latchup cannot be handled in terms of a PAR_{FAIL}. Device ceases to function.

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4.3.2 Burnout Analysis.

Burnout analysis consists of determining the stress on the device and comparing that stress to the failure threshold of the device. However, burnout data in the dose rate environment is not usually readily available, and some procedure for estimating the burnout threshold must be used.

At moderate dose rates, $(\dot{\gamma} < 10^{11}$ rads(Si)/s), burnout seldom occurs because of the energy in the pulse. Rather, burnout occurs because of energy sources in the circuit, (power supplies, capacitors, inductors), releasing their energy in the device. The analysis then must consider the circuit current limiting, device susceptibility threshold and often will use the Wunsch-Bell equation (Ref. 7) or one of its modified forms (Ref. 8), to translate the threshold data to the time regime in question. If the device stress multiplied by the design margin is less than the expected failure threshold, the part is considered safe. If not, then device substitution, or circuit hardening techniques are used.

Existing data bases usually exhibit a wide range of values in the burnout thresholds. These data bases are usually most useful for comparison of devices in the device selection process. For reliable *burnout* data, a number of factors such as, the defined failure criterion, the test techniques, and the data analysis methods must be carefully examined for consistency with the application. If adequate documentation is not available with the data, the data base may be unusable for accurate burnout analysis, and new data may be required.

4.3.3 Latchup Analysis.

Latchup analysis consists of identifying devices which are susceptible to latchup. Some device technologies such as junction isolated integrated circuits are known to be latchup-prone. Other technologies may require formalized latchup analysis procedures (Ref. 9) to identify latchup paths. If latchup paths exist, then some action must be taken. Some of these actions have been discussed earlier, and consist of hardening features like part substitution, or system solutions (Ref. 10).

4.4 DESIGN MARGINS.

There are several design margins which can apply to a system. As previously indicated, the dose-rate design margin is usually a ratio of a mean dose-rate threshold to a specified dose rate. However, there are some exceptions. Typical design margins are given below.

1. For circuits in which the failure probability increases with dose rate, the design margin is

$$DM_{\dot{\gamma}} = \frac{\dot{\gamma}_{MF}}{\dot{\gamma}_{spec}} \quad , \tag{11}$$

where $\dot{\gamma}_{MF}$ is the mean dose rate for failure. An example of this design margin would be the case of upset in integrated circuits.

2. A subset of the first case would apply for circuits that incorporate circumvention in their design. In this case, the design margin would be

$$DM_{\dot{\gamma}} = \frac{\dot{\gamma}_{MF}}{\dot{\gamma}_{CIRC}} \quad . \tag{12}$$

3. For some cases, the failure results from a change in the relative circuit response time. The design margin in these cases may be defined in terms of the allowable transient duration. The design margin could be

$$DM_{\dot{\gamma}} = \frac{t(allowed)}{t(induced)} \quad . \tag{13}$$

The allowed transient duration could be a recovery time in digital circuits or a saturation time in linear circuits.

4.5 DATA REQUIREMENTS.

Radiation response data on devices are needed for various aspects of the design of a radiation hardened system. The requirements on data for the design hardening phase and the hardness assurance phase are somewhat different. These differences are related to the issues of part qualification and part acceptance.

4.5.1 Radiation Characterization.

Dose-rate response data are needed in the design hardening effort to aid in part selection and the determination of expected design margins. The characterization data may be obtained from existing data, or from new part characterization tests.

4.5.1.1 Existing Data. Actual characterization measurements can be avoided if there exists a large body of data describing the dose-rate response of the devices. However, extreme caution must be exercised when existing data are used. Since most dose-rate effects are related to device geometry, diffusion length, doping, etc., assurance must be obtained that the data being used do in fact apply to the device in question.

Existing data sources for burnout data may be considered for use. However, there are a variety of ways in which burnout data may be taken. The test pulse duration and shape, the test circuit, the definition of failure, and the sources of devices are all variables which may affect the data. Burnout threshold data may be useful, provided that the design margin is large enough to make the devices HCC-2 or HNC.

Latchup can be a low probability failure mode in latchup-susceptible devices, and no amount of existing data can establish the latchup susceptibility of a part type with confidence. Latchup is lot sensitive, and existing data generally are not useful except to demonstrate that a particular device has a significant latchup problem.

4.5.1.2 Characterization Tests. Characterization measurements are made on samples of parts to estimate the radiation response of the population of parts. The sample set consists of piece parts of a single part type selected from a procurement lot. It is important to assure that a variety of date codes be represented in the sample in order to obtain a representative device response (Ref. 11). Several situations exist.

Upset Testing. Upset testing is usually nondestructive. Therefore, an upset threshold test on 100% of the devices could be performed, provided that only a small number of state vectors are required to be tested. For large-scale integrated circuits, the number of state vectors which need to be tested may preclude a 100% test because of potential total dose damage to the device, test time and cost. In these cases, the upset threshold must be found on a sample basis.

Burnout Threshold. Burnout threshold measurements are destructive tests. Therefore, sample measurements must be made. The principal difficulty in burnout characterization is that threshold data are quite variable, the tests are time consuming,

and since tests are usually done on small samples, good statistical analysis is not available (see Section 5.3.2).

Latchup. Latchup is a problem which cannot be solved by sampling, since latchup can be a low probability failure mode. Therefore, sample tests are usually inadequate to determine the extent of the problem. As a result, latchup cannot be handled by statistical inference.

Existing data on latchup usually take the form of frequency of occurrence of latchup at some preselected dose-rate screening level. Very little data exist on the dose-rate threshold at which latchup occurs. Yet, it is precisely this threshold information which would be required to perform statistical hardness assurance. Therefore, alternate solutions are needed to handle the latchup problem at the system level, or latchup-free devices must be used.

4.5.1.3 Sample Sizes. It is important, from statistical considerations, that as many devices as practical be used for radiation characterization measurements (Ref. 12). A good statistical test would include at least 25 parts, and more would be better. An absolute minimum would be five parts, with such a small number being used only when the parts are difficult to obtain or the tests are very expensive. A small number of parts could lead to a poor and possibly erroneous characterization. Furthermore, since the criteria for categorizing parts may depend on statistical considerations, the use of a small number of parts may result in devices being categorized as HCC-1 (lot acceptance test required) simply because of wide statistical uncertainties. This situation can lead to the requiring of large design margins, and perhaps greater expense. It is worth noting that a small sample size may turn out to be an "expensive economy."

4.5.1.4 Measurement of Stress to Failure. The recommended procedure for characterization measurements is to measure the threshold dose rate at which the dose-rate effect occurs. Many test methods have been written describing radiation test procedures. A listing of some of these procedures is given in Appendix B.

The general test procedure varies, depending on the effect being measured. However, in almost all cases it is the threshold dose rate at which the dose-rate effect occurs, which is to be measured. The exception to this rule is data taken for burnout effects. This exception will be discussed later.

4.5.1.5 <u>Example of Upset Data</u>. An example of data for CMOS 16K random access memories is shown in Table 2. The data shown are for loss of data measurements performed at a linear accelerator. These data are presented as an example of the calculations described in the previous section, and should not be used for design information. A log normal cumulative plot of the data is shown in Figure 2, indicating the well-behaved distribution of this particular data set. A similar plot would need to be made for each data set in order to assure that the statistics used do, in fact, apply to the data in question.

Table 2. Loss of data parameter measurement.

| Device Serial Number | All 1's | | | |
| | No Upset | | Upset | |
	$(\dot{\gamma})$	$ln(\dot{\gamma})$	$(\dot{\gamma})$	$ln(\dot{\gamma})$
1	8.0 E6	15.89	8.57 E6	15.96
2	7.14 E6	15.78	8.29 E6	15.93
3	8.29 E6	15.93	9.71 E6	16.09
4	8.29 E6	15.93	8.86 E6	16.00
5	1.0 E7	16.12	1.03 E7	16.15
6	1.0 E7	16.12	1.11 E7	16.22
7	1.09 E7	16.20	1.11 E7	16.22
8	1.0 E7	16.12	1.14 E7	16.25
9	1.06 E7	16.18	1.14 E7	16.25
10	1.17 E7	16.28	1.29 E7	16.37
	Avg. $ln(\dot{\gamma}) =$	16.06	Avg. $ln(\dot{\gamma}_{FAIL}) =$	16.14
	Std. Dev. $s_{ln(\dot{\gamma})} =$	0.16	Std. Dev. $s_{ln(\dot{\gamma}_{FAIL})} =$	0.15

The data points representing the lowest upset value for the dose rate have been least square fit for the analysis. Using the lowest upset values may be adequate for data of sufficient quality, where the difference between the highest non-upset dose rate and the lowest upset dose rate is only a few percent (~25%). In other cases, a maximum likelihood estimate could be used (see Reference 13).

The cumulative plot of Figure 2 indicates that the distribution of these data is approximately log normal. Therefore log normal statistics will be assumed to be justified for use for hardness assurance on this device. The log normal mean and standard deviation are calculated in Table 2 for use later in this document. (These parameters are defined in Section 2.)

4.5.2 Nonstatistical Problems - Latchup.

Some dose-rate effects cannot be analyzed statistically. For example, latchup sometimes has such a low occurrence rate that the gathering of statistics about the stress to failure would be impractical. Therefore, in the case of latchup, a less rigorous hardness assurance approach is often used for devices that are latchup prone. The procedure generally follows one or more of the following techniques.

- Latchup analysis
- Latchup screens
- System solutions.

4.5.2.1 <u>Latchup Analysis</u>. A latchup analysis procedure (Ref.9) has been developed for bipolar circuits to aid in the latchup assessment of circuits. The purpose of the latchup analysis procedure is to determine whether the device is latchup free, by using an analytical technique. This procedure seeks out all the four-layer PNPN paths in the device. By use of this procedure, one can determine if four-layer paths exist, and if they are biased correctly for latchup to occur. Presumably, if paths exist but are improperly biased for latchup, the device will not latch up. It should be noted that such analyses are complex and involve considerable time in acquiring the necessary device-design data to perform the analysis.

4.5.2.2 <u>Latchup Screens</u>. When four-layer paths exist in devices, the question of latchup must be considered. It has been suggested that if the beta product of the four-layer path could be determined, latchup could be handled statistically. However, insufficient data exist to qualify this technique, since parasitics are involved and quantification is elusive.

Alternately, latchup screens are often imposed to find latchup-free devices. These screens nondestructively test 100% of the devices in an ionizing radiation source (Ref. 14). All devices which latch are discarded. Problems associated with this technique are discussed in Section 5.2.2.
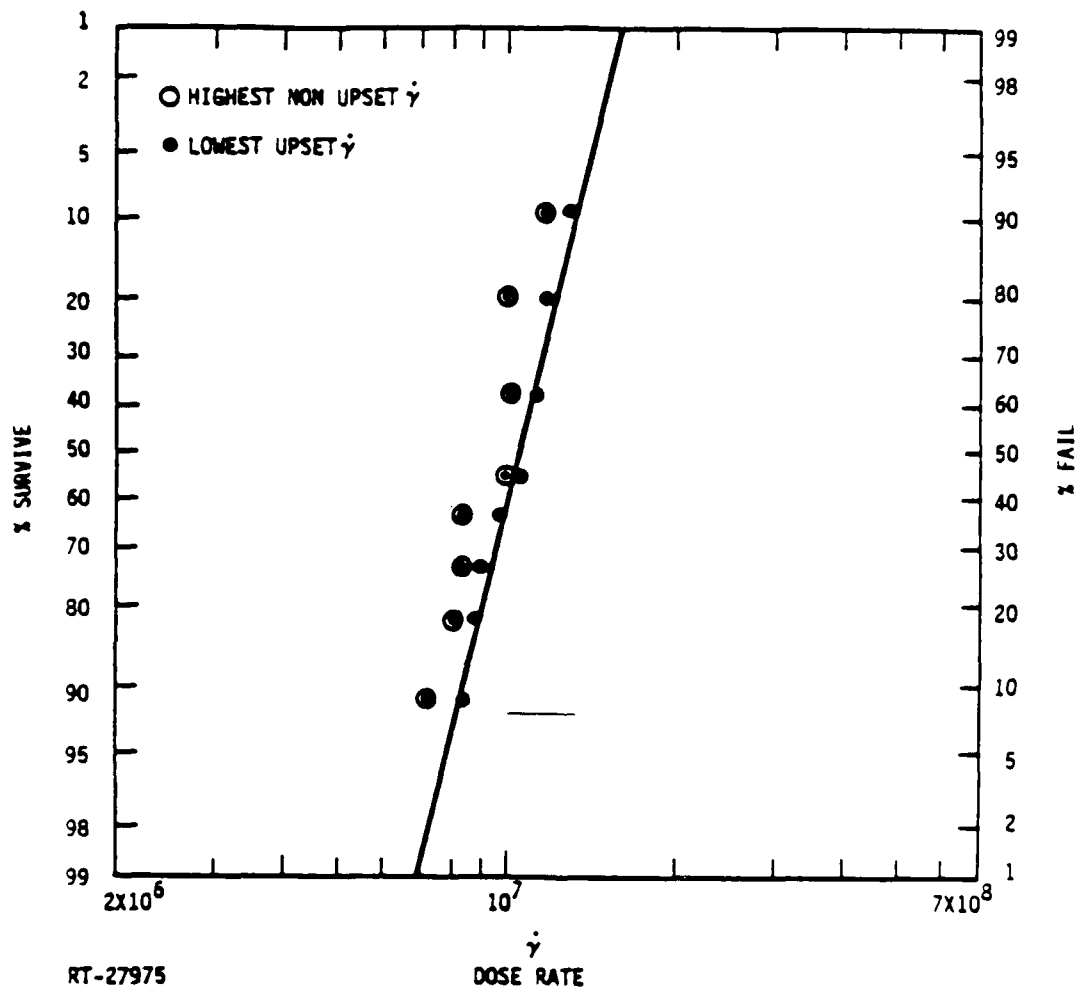
Figure 2. Cumulative log normal plot of upset dose rate for a CMOS memory.

4.5.2.3 System Solutions. Finally, latchup can be handled effectively at the system level. A variety of methods can be used. These methods are not the subject of this document, and thus are not discussed in detail here. However, some of the more effective techniques are:

- Power management, whereby the power to the device is momentarily interrupted, thus interrupting latchup.

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- Current and voltage limiting, where the applied bias and the allowable current are held well below those required for latchup.

In any event, the best solution to the latchup problem is to use devices which are not latchup susceptible whenever possible. Three means of avoiding latchup at the device level are:

- Dielectric isolation, where no more than two active junctions are allowed within an isolated region.

- Process controls to prevent latchup, which reduce the parasitic gains of the four-layer paths to extremely low values. These controls may involve gold doping, neutron radiation, epitaxial layers on highly doped substrates, or sapphire substrates for CMOS devices.

- Analysis which demonstrates that any four-layer paths that may exist cannot latch because of bias or circuit conditions.

4.6 LOT ACCEPTANCE TESTING.

Hardness assurance acceptance tests are performed on devices during the production phase of a program. These tests are usually tests performed on samples from procurement lots of devices in order to assure that the devices procured during production have the same radiation performance as indicated in the characterization tests. Acceptance testing will be discussed in Section 5.

SECTION 5
HARDNESS ASSURANCE

5.1 RADIATION HARDNESS ASSURANCE.

The design margin approach for part categorization is used to determine if hardness assurance lot acceptance testing is required for a particular part type. The two methods used for this categorization are the design margin break point (DMBP) method and the part categorization criteria (PCC) method. Both methods require part characterization data to determine the design margins.

DMBP is generally used for systems with moderate requirements, and in cases where the dose-rate responses of the devices are well understood, or at least are bounded. In this case, the calculated design margin for each piece-part is compared to a specified value, and based on this comparison, the part category is chosen.

PCC applies in all cases where the statistical distribution of failure is known, and is generally used in systems with severe requirements on part survivability. Sometimes a combination of the two methods can be used; that is, DMBP is used to categorize less sensitive parts, and the PCC value is used for the more sensitive parts.

In any application of these hardness assurance methods, a value must be specified which will be used to separate unacceptable and HCC-1 parts. The value must be based on several considerations, such as number of parts rejected, part availability and cost.

5.1.1 Design Margin Break Point Method.

The DMBP method (Ref. 3) is often specified for systems with moderate requirements with respect to the device response levels. The DMBP values are sometimes based on a statistical baseline, but are more often based on good engineering judgement, threat specification levels and system considerations. The DMBP value is the break point between HCC-1M, where acceptance tests are required on each lot, and HCC-2, where tests are not required on each lot. DMBP provides a qualitative level-of-survival probability and confidence level, based on past generic response and engineering judgement. Figure 3 shows the relationship between the break point values.

Dose Rate DM	$\leqslant 2$	$<$ Dose Rate DM	$\leqslant$ DMBP Value	$<$ Dose Rate DM*
Part is unacceptable		HCC-1M part; lot acceptance testing is required		HCC-2 part; lot acceptance testing is not required

Figure 3. Example of relationship between dose-rate DM and DMBP value.

5.1.2 Part Categorization Criteria Method.

The PCC method (Refs 1,2) is generally required for systems in which stringent requirements are placed on part types. When PCC is used, it is necessary to calculate the PCC values based on the characterization data. The PCC data are used to differentiate between HCC-1 and HCC-2 parts. Figure 4 shows this relationship. When the part is judged unacceptable, the corrective action indicated in Section 5.1.3 should be considered.

Dose Rate DM	$\leqslant 2$	$<$ Dose Rate DM	$\leqslant$ PCC Value	$<$ Dose Rate DM*
Part application unacceptable		HCC-1M; lot acceptance testing is required		HCC-2; lot acceptance testing is not required

Figure 4. Example of relationship between dose-rate DM and PCC value.

Before the method used for determining the PCC value is presented, a discussion of the factors used in the calculations is in order. The discussion will include the variability of the dose-rate failure values obtained during characterization, a confidence factor and the required survival probability.

The variability of the data is represented by the standard deviation, s, and is calculated using the $\dot{\gamma}_{FAIL}$ values described in Section 4.2.4. Because the log normal distribution is assumed, $s_{\ell n(\dot{\gamma}_{FAIL})}$, which is the standard deviation of the logarithm of the $\dot{\gamma}_{FAIL}$ values, is calculated as follows.

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*A design margin value should be specified to separate HCC-2 parts from HNC parts.

$$s_{\ln(\dot{\gamma}_{FAIL})} \equiv \left\{ \frac{1}{(n-1)} \sum_{i=1}^{n} \left[\ln(\dot{\gamma}_{FAIL_i}) - \overline{\ln(\dot{\gamma}_{FAIL})} \right]^2 \right\}^{1/2} , \tag{14}$$

where $\dot{\gamma}_{FAIL}$ is the dose rate resulting in failure for the ith device, and n is the sample size.

The level of confidence and the survival probability are introduced into the calculations by multiplying $s_{\ln(\dot{\gamma}_{FAIL})}$ by the one-sided tolerance limit factor K_{TL}, which is selected from a table of one-sided tolerance limit factors (see Appendix C). This factor is a function of sample size n, survival probability P_{DIST}, and confidence level C. For example, 90% confidence in 99% probability of survival means that if the characterization test were repeated many times on different samples from a lot, 90% of the time 99% of the $\dot{\gamma}_{FAIL}$ values would be equal to or greater than the mean less K_{TL} times the standard deviation s, or $\overline{\ln(\dot{\gamma}_{FAIL})} - K_{TL} s_{\ln(\dot{\gamma}_{FAIL})}$, for a log normally distributed variable.

The PCC value is calculated from the following relationship.

$$PCC = \exp K_{TL} \, s_{\ln(\dot{\gamma}_{FAIL})} \quad . \tag{15}$$

Increasing P_{DIST} and C, and consequently K_{TL}, increases the PCC value and the cost of the hardness assurance program, since increasing the value of PCC increases the number of part applications that will be categorized as HCC-1M, requiring expensive lot acceptance testing. Increasing the sample size n generally will increase the cost of the characterization test. However, this added cost may be more than offset during the HA phase of the program, since increasing the value of n results in a lower value of K_{TL}, which in turn may reduce the number of part types requiring lot acceptance testing. As can be seen, the values of P_{DIST}, C and n selected are a tradeoff between the level-of-hardness assurance desired and the amount of funding available for the HA program. The values of P_{DIST}, C and n need to be specified by the SPO when the PCC method is used.

A part type classified as HCC-2 does not require routine lot acceptance testing. However, when the dose-rate margin approaches the PCC value, a sample test should be conducted periodically during parts procurement. It should be noted that a value of 10 is often used as the breakpoint value for HCC-2 when using the DMBP method.

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Nondestructive tests such as dose-rate upset testing may be performed on a 100% screening basis for parts which have been categorized as HCC-1. Table 3 indicates the possible test action which may be required.*

Table 3. Possible testing requirements.

	HCC-1	HCC-2
Upset	100% screen	Periodic lot screen
Burnout	Sample test	Occasional sample test
Latchup	100% screen	Not required

5.1.2.1 An Example of the Use of the PCC Method. If a system has stringent requirements, or if the parts used in the system have failure levels close to the specification level, then a separate decision must be made about the risk to be taken for each part type used. Sometimes, only a few part types are mission critical, and cannot be allowed to fail. Often, certain memories used in the system may not be allowed to upset or to lose data through the radiation event. For these parts, an estimate of the survival probability and the confidence in survival are essential for design hardening.

The reason for the use of the PCC method is that the required design margin is usually lowered from the value used in the DMBP method, since the margin is based on the actual device performance, and not on a worst-case estimate of the performance of a number of device types.

Let us assume that the memory used in Figure 2 is used in a system in a moderate environment. Let us further assume that the requirements for the part are described in Table 4.

The first quantity required for the calculation is the dose-rate design margin. This is determined from the data of Table 2, and the upset level specification.

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*Recently, 100% screening of parts has come under criticism on the basis that the screen may overstress the parts, thus creating latent defects and impacting device reliability. This postulate has not yet been experimentally justified.

The mean failure level is given in Section 4.2.5 as

$$\dot{\gamma}_{MF} = \exp \overline{\ln(\dot{\gamma}_{FAIL})} \quad . \tag{16}$$

Table 4. Requirements at part location.

Specified Threat Level	5 E6 rad(Si)/s
Required-Survival Probability	0.9999
Required Confidence Level	0.9

From the data in Table 2,

$$\dot{\gamma}_{MF} = \exp(16.14) = 1.02E7 \quad . \tag{17}$$

Since the specified threat level is 5E6, the dose-rate design margin is

$$DM_{\dot{\gamma}} = 1.02E7/5E6 = 2.05 \quad . \tag{18}$$

The part categorization criterion, PCC, is obtained from Section 5.1.2. The one-sided tolerance factor, K_{TL}, is obtained from Appendix C; for the appropriate sample size (N = 10), the survival probability (P = 0.999), and the confidence level (C = 0.9).[*]

$$PCC = \exp K_{TL} \cdot s_{\ln(\dot{\gamma}_{FAIL})} \tag{19}$$

$$PCC = \exp(5.538 \times 0.15) = 2.3 \quad .$$

Since the PCC value is larger than the DM , the part is categorized as HCC-1M and lot acceptance tests must be performed.

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[*]Caution must be exercised when extrapolating data to extremely high probability levels.

5.2 HARDNESS ASSURANCE REQUIREMENTS.

The various techniques which can be used for hardness assurance have now been discussed. This section will provide some guidance on how to apply some of these techniques to various systems.

5.2.1 Upset Hardness Assurance.

Either the DMBP or the PCC method could be used for hardness assurance decisions, depending on the required probability of survival and the device technology used. Upset testing may often lead to an adequate statistical determination of thresholds for failure. On therefore, has the option to use a number of different hardness assurance techniques in the application of the PCC and DMBP methods. One can select from:

- Device selection
- Design modification
- 100% screen
- Sample testing
- System solution.

For systems requiring high confidence of survival, a 100% screen may be used to assure the upset survivability of the device with greater confidence. A 100% screen can be an effective technique for integrated circuits at small-to-medium levels of integration. For higher levels of integration, a statistical approach may be used, since the number of state vectors required to be tested may preclude a 100% screen. The cost of a 100% screen can be large, and one must make a tradeoff between the cost of testing each device and the required survivability of the system.

For systems with moderate requirements, the DMBP technique may be the most cost-effective method of achieving the desired confidence in survival. For cases where the design margin is small, the PCC method may be used to determine if lot acceptance tests may be required.

In most cases, a system-level solution for upset can be used. The circuits can be designed to be upset tolerant, and be reset after the pulse of radiation. Devices less sensitive to radiation can be substituted for radiation "soft" devices. In the final analysis, a combination of techniques provides the best solution to the dose-rate hardness assurance problem.

5.2.2 Latchup Hardness Assurance.

Since latchup is often a low probability failure mode, hardness assurance for latchup presents a unique problem. There are very few cases where sufficient statistical data exists to apply the PCC hardness assurance method. In moderate environments, where the dose rate environment is significantly lower than the expected latchup thresholds of the devices, the DMBP method may be used. In any case, alternate hardness assurance techniques must be used. The only techniques available to be used are the following:

- Device selection
- 100% screen
- System solution.

Hardness assurance for latchup is best solved by part substitution or by a system-level solution. Part substitution implies that parts which are not latchup susceptible are substituted for parts which are latchup prone.

There are a number of ways by which latchup-free devices are found. Some of these ways are discussed below.

1. Device Construction

   The use of special processing methods, such as dielectric isolation, buried layers, gold doping, etc., are techniques which are used to prevent latchup. These techniques either eliminate four-layer paths, or assure that the parasitic gains of the devices are too small to sustain latchup.

2. Latchup Screens

   The use of latchup screens attempts to find devices which latch by using a nondestructive radiation screening test (Ref. 14). Devices which latch are eliminated from use in the system. There are a number of significant problems with the use of latchup screens. These problems are discussed later.

3. Latchup Analysis

   Latchup analysis is an attempt to find latchup-prone devices through the analysis of the layout and processing rules used in the device manufacture (Ref. 8). It is usually assumed that devices that have four-layer paths will

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not latch if the current source supplying the path is insufficient to support latchup. Since the four-layer paths are parasitic, one must perform a careful analysis to ensure that the biases and current sources that are present in the non-radiation environment are in fact the correct current and bias sources that are supplying the path during the dose-rate irradiation.

5.2.2.1 Cautions - Latchup.

There are a number of precautions which need to be considered when deciding on latchup hardness assurance techniques. Some of these precautions are discussed below.

1. Latchup Screens. Most latchup tests are performed using a Linac or a flash x-ray facility (Ref. 14). These tests are usually made at a fixed dose, approximately 500 rad(Si), in some specified test configuration. There are a number of problems with this kind of test procedure.

   The first uncertainty is the design of the test configuration. It is necessary to determine the worst-case conditions for the test, and to bias the device properly for the test. The latchup analysis procedure (Ref. 9) is the preferred way to arrive at these worst-case conditions. An arbitrary choice of biases and test configuration can only lead to uncertainty in the test results.

   LSI circuits pose a more complex problem. The problem of proper selection of test vectors for the latchup screen is extremely complex. These circuits may contain more output states than can be practically monitored, and an evaluation of the application of the device in the system in which it is used is the usual way that the test vectors are determined. This, of course, leads to uncertainties in the results of the screening procedure. In these cases, it is often better to power strobe or power interrupt upon detection of a radiation pulse.

   Finally, it is well recognized that latchup in integrated circuits is temperature dependent. The condition of latchup depends on the magnitude of the gain of parasitic transistors in the integrated circuit. These gains are temperature dependent, and may vary by factors of three to four over the operating temperature range. A device which does not latch in a room temperature test may latch in a test at the maximum operating temperature

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(Refs. 14,15). Therefore, the screen must be performed at the maximum device operating temperature in order to be valid.

2. Latchup Windows. The validity of latchup screening procedures has been challenged by the recent discovery of latchup windows (Refs. 16,17). It has been observed that latchup may occur in some devices within a narrow range of doses. The device does not latch above or below this range. A latchup screen will then detect the latchup only if the test dose is fortuitously within this range.

    The latchup window phenomenon has been seen in CMOS devices. In particular, the CD4047, CD4061 and the CD4094 have been observed to have latchup windows. How widespread this problem may be is not yet known. There is no reason to believe that the latchup window problem is limited to CMOS devices. Until further information on the latchup window phenomenon is obtained, latchup screens are subject to question.

3. Latchup Analysis. Latchup analysis seems to be a useful tool in the control of latchup in systems. The latchup analysis procedure (Ref. 9) details the requirements and procedures to perform the analysis and achieve a reasonable confidence in the result. However, the application of the technique requires detailed knowledge of the design rules for the device, and the acquisition of layout information for the device processing.

    The objective of the latchup analysis procedure is to identify all four layer paths in the device, and to make a judgement about whether or not the paths will latch. Obviously, if no paths exist, the device is latchup free. However, if paths are found in the device, the procedure seeks to determine the susceptibility of the paths.

4. Suggested Procedure. A reasonable procedure to follow for latchup hardness assurance is described below for devices.

    The process begins with device selection. The devices are subjected to a latchup analysis procedure to determine whether or not four layer paths exist. Should no paths exist, a high-confidence, latchup-free design can be effected.

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Should four layer paths exist, two options are available. The part may be replaced and the process repeated, or the circuit design may be altered. Should the analysis again determine that a four layer path exists that is properly biased for latchup, two options are possible. The parts may be screened to test for latchup occurrence using test conditions determined from the analysis. This procedure may result in moderate confidence in a latchup-free system. Alternately, a system solution, such as circumvention, may be used to result in high confidence in a latchup-free design. However, power must be removed quickly, within a few microseconds, to prevent burnout in devices.

Should a four-layer path exist, and should the latchup analysis demonstrate that the path is not biased correctly for latchup to occur, one can terminate the process with low to moderate confidence that the system is latchup free. This approach may be feasible and cost effective for the kinds of systems where latchup may be tolerated and operation manually restored.

Alternately, one may improve the system through the use of latchup screens and/or system solutions. This flow is diagrammed in Figure 5.

5.2.3 Burnout Hardness Assurance.

Burnout in the dose rate environment may take on more than one form. The most common failure is junction burnout, occuring as a result of the dose rate radiation. Another burnout mechanism may be the failure of the metallization. Hardness assurance techniques for controlling these effects are considered, at present, to be only tentative and unproven. The matter of burnout in the dose rate environment is still the subject of research, and a complete characterization of the mechanisms is not yet available.

Therefore, the most reasonable choice of a hardness assurance method is the DMBP method. However, the calculation of a design margin break point is complicated by the fact that all burnout conditions are not fully understood. As a result the hardness assurance techniques available are the following:

- Device selection
- Current limiting
- System solutions.
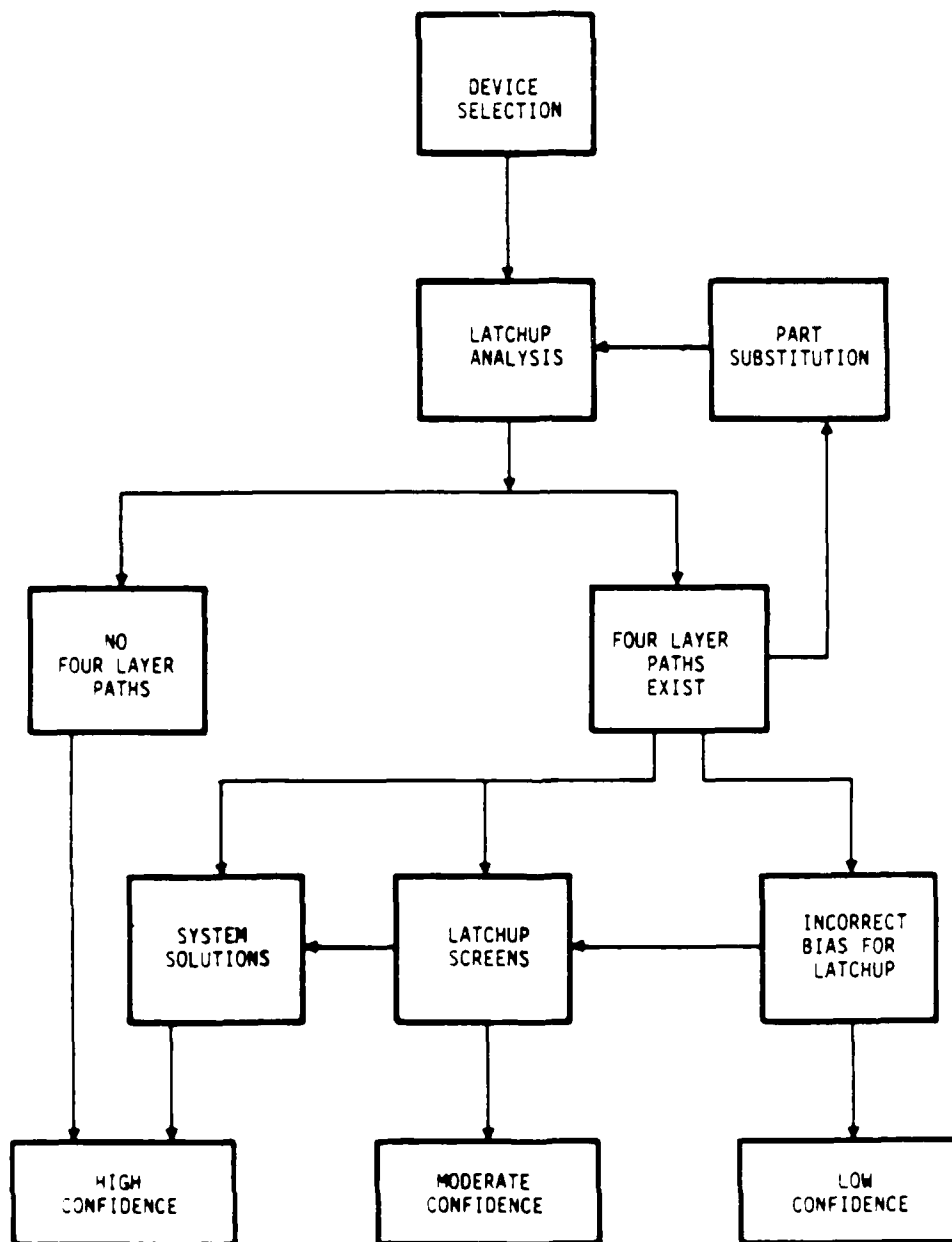
Figure 5. Latchup flow diagram.

These techniques are used to achieve a design margin which is sufficiently large to assure survivability. Since uncertainty exists in the actual burnout threshold of devices, a great deal of judgement and heuristics must be used in the application of the techniques.

1. Device Selection. The use of devices which have higher burnout thresholds is a useful hardness assurance technique. However, since little data are available on burnout in the dose rate environment, pulsed power data are often used to compare the relative hardness of devices. Pulsed power data may provide a meaningful measure of relative hardness for discrete devices and small scale integrated circuits. However, larger scale integrated circuits may have internal failure modes in the dose rate environment which may not be measured by pulsed power techniques.

2. Current Limiting. The most effective hardness assurance technique for burnout hardness is the technique of current limiting. The purpose of current limiting is to prevent any current sufficiently large to cause burnout from flowing into the terminals of the devices. Power supplies, capacitors and input/output terminals are protected with current limiting resistors. A rule which is often used is to provide approximately one ohm of resistance per volt to provide current limiting for all lines connected to an energy source. Input and output leads can be protected to levels to prevent pulsed power burnout at those terminals. Current limiting resistors added for burnout protection are classified HCC-1H.

5.2.3.1 Burnout Hardness Assurance - Cautions. The question of hardness assurance for burnout in the dose rate environment is an extremely difficult issue. The principle difficulty is the fact that very little burnout data exists for devices in the dose rate environment. In fact, available burnout data for devices is often performed using pulsed power techniques, and comparisons are made on the basis of that data.

Unfortunately, the vast majority of the existing data addresses discrete devices. A further complicating factor is that several significant unanswered questions have arisen concerning the existing data. Some of these questions which cause concern are listed below.

● Some devices do not conform to idealized models for device burnout response.

- The distributions of burnout response do not always conform to expected statistical response.

- The burnout response of integrated circuits in dose rate environment may be different than the response predicted on the basis of discrete device pulsed power data.

- The criterion for burnout may differ between devices. No standard test methods exist.

- Synergistic effects affecting burnout are not completely understood.

As a result of these uncertainties, burnout hardness assurance has not been well developed. System hardening techniques will need to be used until many of the unanswered questions have been resolved. Some of these uncertainties are discussed in the following sections in order to provide an understanding of the magnitude of the problem.

1. Idealized Burnout Models.

In many instances, the catastrophic effects of current or power stresses on devices are the significant failure mode for the system. However, the methods used to analyze and obtain design data for the systems do not lead to a great deal of confidence in the analysis.

The power required to burn out a semiconductor junction depends on a variety of factors. Some of these factors are the physical geometry of the device, the impurity profile, the bulk and contact resistance of the device, the polarity and intensity of the applied stress, and a variety of other factors. The point is that although a large number of factors which contribute to the failure of a device have been identified, the burnout problem in devices is not yet completely understood.

Much work has been done to further our understanding of the phenomenon (Refs 6-8,18-21). Some of the most important unanswered questions are:

a. What are the proper test methods for determining failure thresholds and minimizing the scatter in the data?

b. What is the proper statistical distribution which describes the variation of burnout data with stress?

c. What are the measurable, nondestructive, screening parameters which can indicate a device with a low failure threshold?

One of the most common burnout models used in analysis is the Wunsch-Bell power model. This model is an engineering approximation to the physics of the idealized pulsed power burnout phenomenon as it is presently understood.

Initial design of circuitry is usually based on burnout threshold data previously acquired, or new test data obtained specifically for the program. Typically, a sample of devices is tested to provide characterization data where they do not already exist. The tests are usually performed on electrically equivalent unscreened parts.

The failure threshold is usually determined by step-stressing the device using single electrical pulses of increasing power, but of fixed pulsewidth. The device is characterized after each pulse to detect any damage.

The power level increase between pulses becomes a critical factor in the tests. A factor of two increase between pulses is not unusual. Therefore, the uncertainty in the threshold may be as much as 3 dB, simply due to test techniques. A further uncertainty may result in the failure to determine the pulsewidth to burn out properly. The time to burnout may be somewhat less than the pulsewidth of the driving pulser.

For time regimes between tens of nanoseconds and a few microseconds, it is noted that the power required to burn out a junction in reverse breakdown is $K/t^{1/2}$, directly from the Wunsch-Bell equation. This power is absorbed in the junction and bulk resistance giving a current of

$$I_{TH} = \frac{-V_{BD} + (V_{BD}^2 + 4 R_B K/t^{1/2})^{1/2}}{2 R_B} \quad , \tag{20}$$

where

R_B is the device bulk resistance

V_{BD} is the junction breakdown voltage

K is the Wunsch-Bell damage constant

t is the rectangular pulsewidth.

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Measured values of K are recommended to be used. However, when quality data are not available, the values of K are usually derated according to some derating scheme. One such scheme is shown in Table 5 (Ref. 3).

Table 5. Derating factors for Wunsch-Bell damage constants.

Source	Derating
Reliable, well-documented data	1/3
Similar part test data	1/10
Calculated data	1/50

For parts which are characterized for the system in which they are to be used, another modification of the Wunsch-Bell equation is often made. The test data are least-squares fit to the equation:

$$P = At^B ,$$

(21)

where P is the power, t is the pulse duration and A and B are constants found by the least-squares fit. Then this curve is used to find the failure threshold at the expected pulsewidth. Once the derated current is found and the damage threshold is determined, then the circuit currents are limited to yield a desired design margin.

All of the approaches presently used make certain basic assumptions and use similar extrapolation methods. For example, the Wunsch-Bell engineering model is commonly used. It is often necessary to extrapolate the burnout data to pulsewidths of interest, and the simple power law seems to be a convenient way to perform this extrapolation.

There are a number of areas which must be discussed in assessing these analysis techniques:

a. Statistics of the burnout threshold
b. Extrapolation using the Wunsch-Bell power law
c. Combined environmental effects.

2. <u>Statistical Analysis</u>. Burnout testing of devices has yielded very little in the way of information on the statistical distributions describing burnout data. If the statistical distribution is known, derating part data for the statistical uncertainties resulting from small sample data is a straightforward application of confidence bounds. The techniques outlined previously using one-sided tolerance limits can be modified to whatever distribution is used. On the other hand, without knowledge of the statistical distributions, any derating scheme is subject to question.

A number of authors have attempted to study and describe the statistical distribution of burnout data. Typical of these efforts are the works of Egelkrout (Ref. 6) and Alexander et al. (Ref. 19).

The most commonly used distributions are the normal and log normal distributions. Egelkrout set out to examine the lot-to-lot variability of burnout data, and attempted to show that existing data analysis methods and the statistics used result in inadequate design margins. He also tested several trial distributions against existing data to determine the proper statistical distribution. He postulated that burnout data may follow a Weibul distribution rather than the usual log normal. Egelkrout does, in fact, show that the statistical problem is not yet solved. Perhaps more careful test procedures and use of confidence limits in the statistical extrapolation may result in a more realistic estimate of useful margins.

Alexander, et al., attempted to develop failure threshold information by testing large numbers of transistors. A number of transistor topologies were used in the experiment to provide the variety of shapes and sizes commonly used in aeronautical systems. A number of common statistical distributions were tested to determine which distribution would be most useful for failure threshold analysis. They found that no single distribution was universally applicable to their data.

The point to be drawn from this is that the use of any statistical procedure based on the failure threshold for devices leads to some degree of uncertainty. Without an adequate statistical description, the extrapolation from sample data cannot be made with confidence. Most often, what is done is that a particular distribution is judged to be acceptable from an engineering point of view, and is used on that basis.

It may be useful to examine the burnout threshold variability from a nonparametric perspective. The designer may wish to know the number of standard deviations from the mean which are required to bound the failure threshold. If the failure threshold can be bounded to within an acceptably small limit, then a suitable design margin can be chosen.

3. Extrapolation. Burnout data are most often measured using one or two stressing pulsewidths. Should the pulsewidth of interest not be the same as the measurement stress, the data will have to be extrapolated, or interpolated in order to provide failure thresholds at the required pulsewidth.

Extrapolation using the idealized power laws can lead to errors since the idealized power laws apply only to limited time regimes or pulse widths. Extrapolation to pulsewidth outside of the region of applicability can lead to very significant errors. In addition, the uncertainty of the data on which the extrapolation is made contributes to the error.

4. Combined Environments. There is some concern about the combined effect of nuclear environments, particularly in the area of burnout. There may be a combined effect should the dose-rate effect occur simultaneously with the incidence of an electrical overstress. This problem has been studied by some researchers, with varying degrees of success (Refs 20,21). The results of the studies seem to indicate that current limiting of devices serves to effectively control combined effects for most digital and analog devices. High power devices, where current limiting is difficult, may be subject to combined effects, and testing in the dose-rate and pulsed power combined environment may be required.

5.3 LOT ACCEPTANCE TESTING.

During the production phase of a program, it is assumed that the parts which are to be used have been characterized and categorized during the design phase. The most cost-effective approach to piece-part hardness assurance is to determine the part requirements during the design phase, and then to use the same requirements for all

future hardness assurance part procurement activity. Therefore, the hardness assurance design documentation (HADD) must include all the information needed to implement hardness assurance procedures.

As previously indicated, parts which are categorized as HCC-1M require lot acceptance testing before use in the system. For dose-rate effects, the hardness assurance lot acceptance tests may take a number of forms. They may be 100% tests of the lot (screens), or they may be sample tests. The 100% screens may apply only to some upset and latchup tests, and will be discussed later. Alternately, some tests for upset and most burnout tests can be destructive, and therefore must depend on sample tests.

Two general methods may be used for lot acceptance tests. The first is called an attribute sampling test method or, more commonly, a lot tolerance percent defective (LTPD) test. This method specifies how many devices out of a given sample size can fail under a given test condition, and still meet an acceptance criterion. A description of this method is given in Appendix C. The LTPD method is widely used for quality assurance. It is simple to use, but requires inordinately large sample sizes when low *failure probabilities with a high* level of confidence are needed. For example, to allow prediction of a failure probability of 1 in 10^4 at 90% confidence, about 2,000 sample parts would have to be tested with no failures. An exception to these comments is that it may be possible to obtain high survival probabilities with a small sample size by performing an LTPD test at several times the specification dose rate (Ref. 12); the extrapolation to higher survival probabilities at the specification fluence requires a knowledge of the probability distribution.

The second method, called a variable sampling test method, determines the statistical behavior of a variable (e.g., dose-rate upset threshold) under test conditions. This method has the advantage of being able to predict a low failure probability, with high confidence, on the basis of a relatively small sample size. It has the disadvantage that it requires assumptions about the probability distribution of the variable involved. Such assumptions are usually reasonable, however, and the advantage of being able to use sample sizes which are easily attainable far outweighs any disadvantages.

5.3.1 Upset Testing.

Upset testing is usually considered to be nondestructive, and therefore can sometimes be imposed as a 100% screen on devices used in a system. However, a 100% screen is not always the solution to assuring hardness.

There are several factors to consider when upset tests are performed. For example, if the device is a combinational logic device, the device may spontaneously recover from upset within some recovery time. One therefore may be concerned with either the upset level or the recovery time for the device, depending upon whether or not the circuit in which it is used is designed to be upset tolerant. Should the device be a sequential logic device, the state may be restored only through reinitialization after the radiation pulse. In this case, the upset level may be the parameter of importance. On the other hand, recovery time may be the parameter of interest, particularly for linear devices, which may saturate when exposed to the dose-rate environment.

In all cases, the number of pulses required to determine the upset level contributes to the total dose exposure of the device. The total dose exposure may be particularly important for MSI or LSI devices where large numbers of state vectors may need to be tested. These cases may again force the use of sample tests.

5.3.1.1 <u>Nondestructive Tests - Screens</u>. The radiation characterization tests and the required circuit upset tolerance will determine the survivability level required for devices. For less complex devices, a 100% test of the devices at the required level may be sufficient to qualify the part. The total dose accumulation and the overstress of the devices subjected to the 100% screen are factors which will need to be considered when deciding on screening tests for the devices.

5.3.1.2 <u>Destructive Tests - Acceptance Tests</u>. In some cases, the devices may be damaged in determining either the upset threshold or the survivability level. In these cases the tests must be performed on samples and the appropriate procedures used for lot acceptance. An adequate sample size, consistent with a desired confidence and survival probability, must be chosen see "Piece Part Neutron Hardness Assurance Guidelines" (Ref. 1), and Appendix B .

5.3.2 Burnout Tests.

The acquisition of data to assess the burnout susceptibility of devices in the dose-rate environment presents a unique situation. Burnout characterization tests are seldom performed in the dose-rate environment. The burnout or damage levels whereby devices are compared are usually determined by pulse power testing of the device to failure. Therefore, burnout tests are always sample tests and statistical inference must be made.

5.3.2.1 Pulsed Power Tests. Most burnout tests are performed by applying an electrical overstress to the device, and measuring the stress to failure for a given pulse duration. There are obvious problems associated with this method of measurement. Some of these are: (1) the pulse duration; (2) failure statistics; and (3) correlation with dose-rate-induced burnout mechanisms.

The pulse power tests are usually performed at some pulse duration comparable to the expected duration of the dose-rate-induced photocurrent. The power to failure is usually assumed to follow the Wunsch-Bell power law (Ref. 7), for time regimes between approximately 100 ns to a few microseconds,

$$POWER_F = K \, t^{-1/2} \quad , \tag{22}$$

which allows the extrapolation of the failure power (P_F) to times comparable to the photocurrent pulse duration.

Statistical analysis is usually performed using log normal statistics on the stress to failure and acceptable design margins are applied. The choice of log normal statistics is a convenient choice, but perhaps not entirely correct. It is convenient because it provides a consistent approach. However, the question of correct governing statistics has not yet been settled (Ref. 6, 16, 17).

The use of the log normal statistics allows the application PCC method with its mathematical formalism. Another approach which is sometimes used is to determine the failure threshold for devices by data analysis and to apply a derating factor based on engineering judgement. In this way, a DMBP value may be chosen, and the DMBP method applied.

5.3.3 Latchup Tests.

Latchup can be a low probability failure mode, and therefore is impractical to approach using sample statistics. The usual hardness assurance test applied to latchup-prone devices is a latchup screen. The screen is applied to 100% of the devices, and all devices which latch are rejected from use in the system (Ref. 14).

There are significant problems with the use. of a latchup screen. Possible uncertainties in the screening tests suggest that system-level solutions should be used if latchup-prone devices cannot be eliminated from the design. The uncertainties and cautions to be observed are discussed in Section 5.2.2.1.

SECTION 6
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APPENDIX A
DOSE-RATE EFFECTS

A.1 DEVICE PHOTORESPONSE.

The principal dose-rate effect in semiconductor junctions is the generation of photocurrents. The photocurrents arise in devices when high-energy particles such as gamma rays, x-rays or electrons are absorbed and create excess electron-hole pairs in the material of the device. The collection of these excess carriers by the device junction results in current flow in the device.

The theory of junction photocurrents is well understood, and can be calculated for most normal ionization sources and simple device geometries (Ref. A1). For an incident dose-rate pulse, the transient photocurrent collected by a PN junction is approximately:

$$I_p = q \, g \, A \dot{\gamma} \, W \left[L_p \, \mathrm{erf} \left(\frac{t}{\tau_p} \right)^{1/2} + L_n \, \mathrm{erf} \left(\frac{t}{\tau_n} \right)^{1/2} \right] \quad , \tag{23}$$

where

    q is the electron change

    A is the junction area,

    W is the width of the junction depletion region,

    L_n is the minority carrier diffusion length of electrons in p material,

    L_p is the minority carrier diffusion length of holes in n material,

    is the corresponding minority carrier lifetime, and

    g is the carrier generation rate.

$$g = 4.2 \times 10^{13} \text{ hole-electron pairs/cm}^3\text{-rad(Si)} \quad ,$$

where $\dot{\gamma}$ is the radiation dose rate in rad(Si)/s. A similar decay occurs at the termination of the pulse.

For a radiation pulse which is long with respect to the minority carrier lifetime, the photocurrent reaches a steady-state value of:

$$I_p = q \, Ag(W + L_p + L_n) \dot{\gamma} = q \, Ag \, L_{eff} \dot{\gamma} \tag{24}$$

where L_{eff} is the effective minority carrier collection length around the PN junction. L_{eff} is the sum of the depletion layer width and the diffusion lengths on each side of the junction.

A.2 DOSE-RATE FAILURE.

The photocurrent dose-rate transient failure threshold for a given circuit is normally defined as the radiation level required to produce an output voltage which is sufficiently large to cause a change of state in subsequent logic stages. For small-scale integration, this output voltage may be measured directly for single gates. For larger scale integration, this change may be measured as either a permanent or transient change of state of a cell within the device. This response can cause a logic change or a loss of memory, depending on the type of device being tested.

Sequential logic will typically change state, while combinational logic will usually experience a transient upset and recover after the radiation pulse.

A.3 CORRECTIVE ACTION.

The photocurrent generation in devices acts as an internal current generator in parallel with each of the PN junctions in the device. The problem in hardening devices to dose-rate effects is to eliminate, reduce, or to compensate for the unwanted photocurrents. Some of the major techniques which are used are (Ref. A3):

1. Minimize the number of reversed biased junctions in order to reduce the photocurrent.

2. Increase the operating current density in the device by decreasing the junction area, or by increasing the operating current.

3. Minimize the collection depth in order to reduce the collection volume.

4. Compensate for the photocurrents which flow by adding semiconductor elements to the circuit.

The first technique can be achieved by the use of such techniques as dielectric isolation and thin-film resistors in device construction. The goal is to have no more than two junctions in any conduction area.

The second technique reduces the relative amount of photocurrent with respect to the device operating current. Since the photocurrent is area dependent, one method of increasing the current density is to reduce the device junction size.

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The third method can be implemented by reducing the lifetime in the collection region of the device by use of some lifetime killing method such as gold doping. The collection volume can also be reduced by the use of very thin layers on insulating substrates, such as in dielectric isolation or the use of sapphire substrates.

The fourth method places semiconductor junctions across the base emitter junction of devices in order to shunt the generated photocurrents away from the device base region. In this way, the photocurrent does not cause unwanted voltage drops in the devices, and does not undergo amplification by the active devices in the circuits.

A.4 TRANSIENT UPSET HARDNESS.

Typical transient upset thresholds for several technologies are shown in Figure 6. It should be noted that there may be considerable variation in the upset threshold for various members of a family of devices within a technology type. Any one family within a technology may cover the entire range shown (Ref. A4).

Some general observations can be made. TTL devices seem to have comparable upset thresholds regardless of the level of integration. NMOS is the most sensitive technology for transient upset, while CMOS seems to be the second most sensitive technology. CMOS/SOS, on the other hand, exhibits a high threshold level for upset, because of the reduced collection volume for photocurrents.

Typical latchup thresholds for these families of devices are shown in Figure 7. Latchup is a phenomenon which is very much device dependent, as well as technology dependent. The incidence of latchup in bulk CMOS is high, while the incidence in some families of TTL devices is extremely low.
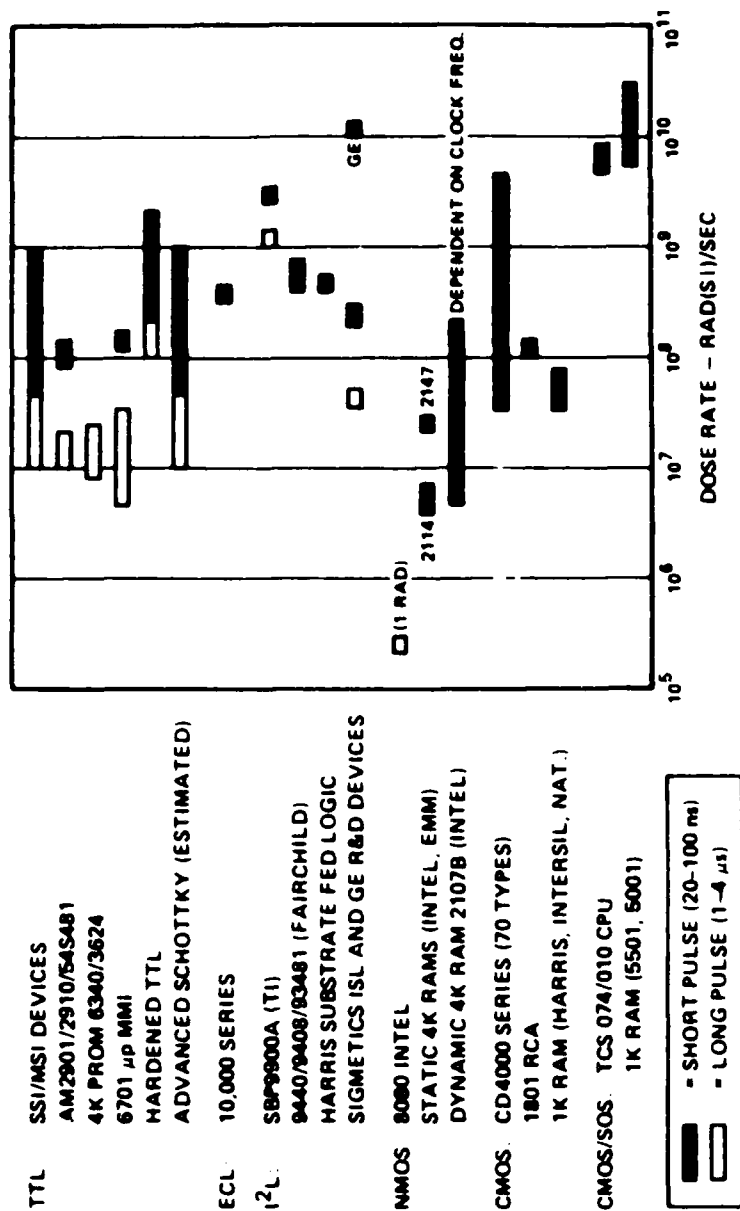
Figure 6. Transient upset hardness (Ref. A4).

PULSE
WIDTH

4 μs
20 ns
20 ns
300 ns

50 ns

3 ns

25°C

110°C

3 ns
10V

20 ns
5V

150 ns
20 ns

10^7 10^8 10^9 10^{10} 10^{11}

DOSE RATE — RAD(Si)/SEC

TTL   6701 μp MMI (1976)
        82S100 FPLA MMI (1978)
        82S11 1K RAM SIGNETICS (1979)
        EARLY 54LS153
        HUNDREDS OF THOUSANDS OF SSI/MSI UNITS TESTED WITHOUT
        LATCHUP
        HARDENED TTL   LATCHUP PREVENTED BY DIELECTRIC
        ISOLATION

ECL   LATCHUP NOT OBSERVED (LIMITED TEST DATA)

I²L   LATCHUP PREVENTED BY LOW SUPPLY VOLTAGE

NMOS   NO PNPN PATHS FOR LATCHUP

CMOS • CD4000 SERIES (70 TYPES, 40 LATCHED) 10V
        NEUTRON IRRADIATED CD4000 (NO LATCHUP – 70 TYPES, 10V)
        CDP 1802 μp (RCA)
        6508 1K RAM (HARRIS, INTERSIL) 5V

CMOS/SOS   LATCHUP PREVENTED BY SAPPHIRE ISOLATION

LINEAR ICs   SOME PART TYPES EXHIBIT LATCHUP

•USE OF GOLD DOPING OR EPI STRUCTURE ALSO
 HAS POTENTIAL TO PREVENT LATCHUP

☐ = RANGE OF OBSERVED LATCHES
☐ = OBSERVED LATCHUP THRESHOLD

Figure 7.   Latchup thresholds (Ref. A4).

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APPENDIX B
DOSE-RATE TESTING

B.1 RADIATION TESTING.

The most common radiation sources which are used for dose-rate testing of semiconductor components are the linear accelerator (Linac) or the flash x-ray (FXR) machine. Because of the wide variety of components, and much wider variety of ways that a component may be used in a circuit, a radiation test plan and report are required for the proper documentation and performance of the tests. Except for dosimetry, test details will vary from device to device.

In general Linacs are useful for testing devices in dose-rate ranges from 1×10^6 to 1×10^{11} rad(Si)/s, with variable pulsewidths. FXR machines can often achieve higher dose rates; however, a given FXR machine can test only at a single pulsewidth.

B.2 CAUTIONS.

There are a number of test variables which must be considered when dose-rate tests are performed. Clearly, good engineering practice must be exercised, and correct radiation test procedures must be followed. Some of the test concerns are listed below (Ref. B1).

B.2.1 Air Ionization.

The radiation pulse can cause air ionization which can result in a spurious component of the measured signal. The presence of these signals can be checked by irradiation of the test fixture without the device being installed.

B.2.2 Secondary Emission.

Charge emission from, or charge injection into, the test device and test circuit can also result in a spurious component of the measured signal. In contrast to air ionization, secondary emission effects are generally not field dependent, and, therefore, it is possible to separate the two effects. Secondary emission can be reduced by shielding the surrounding area and irradiating the device only.

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B.2.3 Orientation.

The effective dose to the semiconductor device can be altered by orientation. Severe dose gradients in a radiation field, along with package shielding may result in nonuniform, and even unknown, doses in regions of the devices. Care must be taken in the positioning of devices in the radiation field.

B.2.4 Dose Enhancement.

High atomic number material near the active regions of the test device can cause an enhancement of the dose delivered to sensitive regions of the device when the device is irradiated at an FXR. The effect is FXR energy dependent, increasing with lower energies. The extent of this effect must be considered in any FXR dose-rate testing.

B.2.5 Noise.

Most pulsed radiation facilities are inherent sources of r-f noise. Such noise minimizing techniques as single-point ground, filtered power supply lines, etc., must be used when attempts are made to make quality data measurements through the radiation pulse.

B.2.6 Dosimetry.

Accurate dose-rate monitors for dose-rate testing are not readily available. Generally, the total dose delivered in each pulse is measured along with some type of measurement of the pulse shape. The dose rate is then calculated. Good dosimetry practice must be used in order to provide adequate dose-rate values (Refs. B2 and B3).

B.2.7 Temperature.

Many dose-rate effects are temperature sensitive. A notable example is latchup in integrated circuits. The temperature during the test should be controlled, and at times, a correct test temperature must be chosen.

B.2.8 Total Dose.

Some dose-rate effects, such as upset, are generally nondestructive to the device. Therefore, some devices may be screened on a 100% basis to determine the upset threshold. However, each pulse of the radiation source imparts some total dose to the

device. For devices very sensitive to total dose, or for very complex devices, the accumulated total dose delivered to the device during dose-rate testing may alter the response of the device, or cause total dose failure. Care must be taken to ensure that the total dose delivered to the device during dose-rate testing does not cause damage to the device which can mask the dose rate effects.

B.3 OTHER DOCUMENTS.

Several standard methods and standard practices have been developed for use in measuring the ionizing radiation environment. These documents should be consulted when radiation tests are performed.

ASTM E 666-78   Standard Method for Calculation of Absorbed Dose from Gamma or X Radiation.

ASTM E 668-78   Practice for the Application of Thermoluminescence-Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices.

ASTM E 820-825   Standard Practice for Determining Absolute Absorbed Dose Rates for Electron Beams.

ASTM F 448-80   Standard Method for Measuring Steady-State Primary Photocurrent.

ASTM F 526-77   Method of Dose Measurement for Use in Linear Accelerator Pulsed Radiation Effects Tests.

Copies of these documents may be obtained from ASTM, 1916 Race Street, Philadelphia, Pennsylvania 19103.

A number of test methods are available in the Military Standards System. Some of these are:

Method 1020, "Radiation-Induced Latchup Test Procedure," (Ref. C3).

Method 1021, "Dose Rate Threshold for Upset of Digital Microcircuits," (Ref. C3)

Method 1023, "Dose Rate Response of Linear Microcircuits," (Ref. C3).

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B3. "Method of Dose Measurement for Use in Linear Accelerator Pulsed Radiation Effects Tests," ASTM E 526.

APPENDIX C
ONE-SIDED TOLERANCE FACTORS

C.1 OVERVIEW.

Hardness assurance applications generally involve statistical techniques to determine the adequacy of design margins in achieving required survival probabilities. The statistical question is addressed well in Appendix E of DNA 5910F, "Piece Part Neutron Hardness Assurance Guidelines for Semiconductor Devices" (Ref. C1), and should be consulted for questions involving statistics.

The purpose of this appendix is to present some of the techniques necessary for dose-rate hardness assurance. A complete treatment is not given, only the information required to use this document is presented.

C.2 SAMPLING.

Most hardness assurance techniques require some sort of sampling and statistical extrapolation to the parent population. The results of sampling are most frequently reported in terms of a confidence, C, that at least a proportion, P, of the lot will not fail under actual test (Ref. C1).

Two kinds of test are often performed on the selected sample to determine the population characteristics. The first is termed "sampling by attribute." In sampling by attribute, some characteristic of the item is monitored. For example, upset testing at a single dose rate would determine whether or not the semiconductor devices within a selected sample of devices would upset or not at that dose rate. This would be a "go-no-go" situation. Either the device upset or not at the particular dose rate. No information would be obtained on the exact threshold for upset or the distribution of the threshold for upset. This kind of test is often handled by using the method of Lot Tolerance Percent Defective (LTPD) (Ref. C2), to make predictions about failure probabilities.

The second method of sampling is termed "sampling by variable." In this case, a measurement is made of some critical parameter in a sample. For example, the upset threshold of each semiconductor device in a sample may be measured in terms of the threshold dose rate for upset. Sampling by variable lends itself well to the application of statistical techniques, provided the statistical distribution of the data is known.

For hardness assurance applications, normal and log normal statistics are often used (Ref. C1). A check should always be made to see if the application of a particular statistical distribution to the data is proper. Most often, for radiation effects, the log normal distribution is assumed, even though the actual distribution of data is not known. There is evidence that even if the log normal distribution is not exactly correct, its use can still provide good engineering approximations to the hardness assurance problem. The log normal distribution is one where the logarithms of the quantities are distributed normally.

C.3 SAMPLING BY VARIABLES - ONE-SIDED TOLERANCE LIMITS.

One statistical technique used with sampling by variable data is the method known as the one-sided tolerance limit. If a parameter is known to be normally distributed, then the estimates of lot quality can be obtained with extremely small samples. Thus, if the parameter, x, is normally distributed (x may be the logarithm of a parameter), and n items are sampled, then a lot is rejected if the limiting quantity, L, exceeds a value, L_{MAX}, where

$$L = m + K_{TL} (n,C,P)s \quad , \tag{25}$$

where

$\quad$ m is the measured mean of the sample,

$\quad$ s is the standard deviation of the sample,

$\quad$ C is the required confidence level, and

$\quad$ P is the required survival probability, or lot quality.

The one-sided tolerance limit, K_{TL}, is a function of the sample size, n, the confidence, C, and the lot quality, P. The statistical statement that can be made is that if more than the proportion, P, devices of the parent distribution has values of x less than L_{MAX}, then the lot will be rejected with probability, C (Ref. C1). L_{MAX} may be a parameter selected such that if its value is exceeded, then failure will occur.

In many hardness assurance applications, the critical parameter may be a minimum and not a maximum. The formulation is similar, and a lot is rejected if the quantity, L, is less than L_{MIN}, where

$$L = m - K_{TL} (n,C,P)s \quad , \tag{26}$$

where the quantities have been previously defined. In this case, L_{MIN} may be a parameter value, selected such that if the actual value falls below this value, system failure will occur.

Table 6 is a table of one-sided tolerance factors for some of the most frequently used lot qualities and 90% confidence. For a complete discussion of these issues, Reference C1 should be consulted.

Table 6. One-sided tolerance limits, K_{TL}.

N	$C = 0.9$				
	P				
	0.9	0.95	0.99	0.999	0.9999
3	4.259	5.311	7.340	9.651	11.566
4	3.188	3.957	5.438	7.129	8.533
5	2.742	3.400	4.666	6.111	7.311
6	2.493	3.091	4.243	5.555	6.645
7	2.332	2.894	3.972	5.202	6.222
8	2.218	2.755	3.783	4.955	5.927
9	2.133	2.649	3.641	4.771	5.708
10	2.065	2.568	3.532	4.628	5.538
11	2.011	2.503	3.443	4.514	5.402
12	1.966	2.448	3.371	4.420	5.290
13	1.928	2.403	3.309	4.341	5.196
14	1.895	2.363	3.257	4.273	5.116
15	1.867	2.329	3.212	4.215	5.046
16	1.842	2.299	3.172	4.164	4.986
17	1.819	2.272	3.137	4.119	4.932
18	1.800	2.249	3.105	4.078	4.884
19	1.781	2.228	3.077	4.042	4.841
20	1.765	2.208	3.052	4.089	4.802
21	1.750	2.190	3.028	3.979	4.766
22	1.736	2.174	3.006	3.952	4.734
23	1.724	2.159	2.987	3.926	4.704
24	1.712	2.145	2.969	3.903	4.677
25	1.701	2.132	2.952	3.882	4.651
30	1.657	2.080	2.884	3.794	4.546
35	1.623	2.041	2.833	3.729	4.470
40	1.598	2.010	2.793	3.678	4.411
45	1.575	1.986	2.761	3.638	4.363
50	1.559	1.965	2.735	3.605	4.324
60	1.532	1.933	2.694	3.552	4.262
70	1.511	1.909	2.662	3.513	4.215
80	1.494	1.890	2.637	3.482	4.178
90	1.481	1.874	2.617	3.456	4.148
100	1.470	1.861	2.601	3.435	4.124

Factors K_{TL} such that with confidence, C, at least a proportion, P, of a normal distribution will be less than

$$m + K_{TL}s \quad . \tag{27}$$

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    ATTN A R TOMME

MARTIN MARIETTA CORP
    ATTN W GAYNOR

MARTIN MARIETTA DENVER AEROSPACE
    ATTN H ANDERSON

MCDONNELL DOUGLAS CORP
    ATTN D L DOHM
    ATTN M STITCH
    ATTN R L KLOSTER

MESSENGER, GEORGE C
    ATTN G MESSENGER

MISSION RESEARCH CORP
    ATTN C LONGMIRE

MISSION RESEARCH CORP
    ATTN R PEASE

MISSION RESEARCH CORP
    ATTN J LUBELL
    ATTN R CURRY

MISSION RESEARCH CORP, SAN DIEGO
    ATTN J RAYMOND

MITRE CORPORATION
    ATTN M FITZGERALD

MOTOROLA, INC
    ATTN A CHRISTENSEN

MOTOROLA, INC
    ATTN L CLARK

NATIONAL SEMICONDUCTOR CORP
    ATTN F C JONES

NEW MEXICO, UNIVERSITY OF
    ATTN DR NEAMEN

NORTHROP CORP
    ATTN J SROUR

NORTHROP CORP
    ATTN E KING

PACIFIC SIERRA RESEARCH CORP
    ATTN H BRODE, CHAIRMAN SAGE

PHYSICS INTERNATIONAL CO
    ATTN J SHEA

R & D ASSOCIATES
    ATTN C KNOWLES

RAND CORP
    ATTN C CRAIN
    ATTN P DAVIS

RAND CORP
    ATTN B BENNETT

DEPT OF DEFENSE CONTRACTORS (CONTINUED)

END

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